

# Compal Confidential

## KHLB2 Schematics Document

Intel Mobile Penryn uFCPGA with Cantiga\_PM + DDRIII + ICH9M

2009-01-19

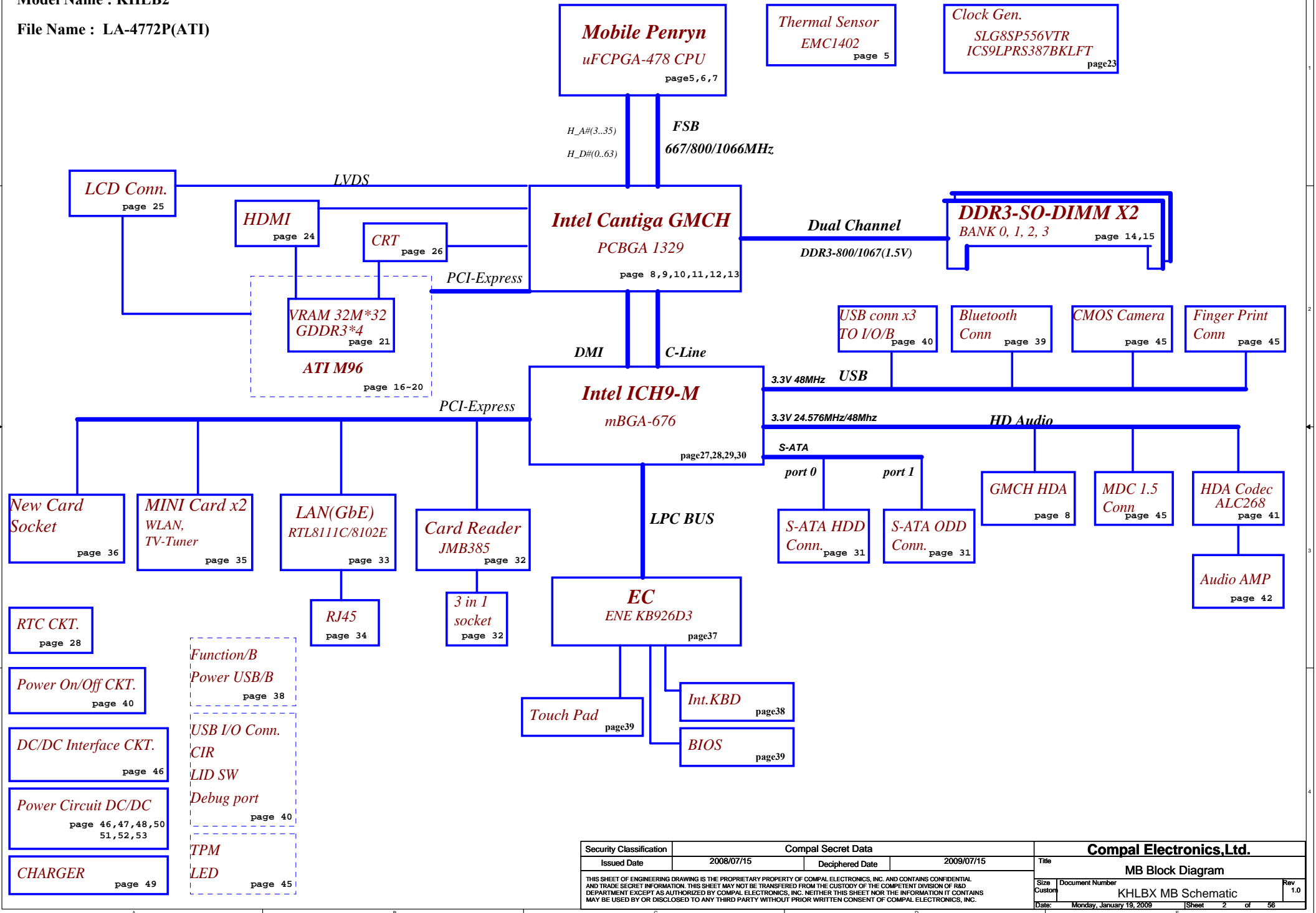
REV:1.0

|   |            |                    |            |                                |                                       |
|---|------------|--------------------|------------|--------------------------------|---------------------------------------|
| Security Classification   |            | Compal Secret Data |            | Compal Electronics,Ltd.        |                                       |
| Issued Date   | 2008/07/15 | Deciphered Date    | 2009/07/15 | Title<br>Cover Sheet           |                                       |
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|   |            |                    |            | Date: Monday, January 19, 2009 | Sheet 1 of 56                         |
|   |            |                    |            | Rev<br>1.0                     |                                       |

# Compal Confidential

Model Name : KHLB2

File Name : LA-4772P(ATI)



|   |                    |                    |            |                          |  |
|---|--------------------|--------------------|------------|--------------------------|--|
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| Size  | Document Number    | Rev                |            | 1.0                      |  |
| Custom  | KHLBX MB Schematic | Date:              |            | Monday, January 18, 2009 |  |
| Sheet   |                    | 2                  |            | of 56                    |  |

DDR3 Voltage Rails

| <div>power plane</div> <div>State</div> | +B | +5VALW<br><br>+3VALW | +1.5V<br>+1.8V<br>+0.75V | +5VS<br>+3VS<br>+1.5VS<br>+1.1VS<br>+VCCP<br>+CPU_CORE<br>+VGA_CORE<br>+1.8VS |
|---|----|----------------------|--------------------------|---|
| S0                                      | ○  | ○                    | ○                        | ○   |
| S1                                      | ○  | ○                    | ○                        | ○   |
| S3                                      | ○  | ○                    | ○                        | ✗   |
| S5 S4/AC                                | ○  | ○                    | ✗                        | ✗   |
| S5 S4/ Battery only                     | ○  | ✗                    | ✗                        | ✗   |
| S5 S4/AC & Battery don't exist          | ✗  | ✗                    | ✗                        | ✗   |

EC SM Bus1 address

| Device           | Address     | Device   | Address     |
|------------------|-------------|----------|-------------|
| Smart Battery    | 0001 011X b | EMC 1402 | 100_1100X b |
| EEPROM(24C16/02) | 1010 000X b | ATI M96  |             |

EC SM Bus2 address

GPIO PIN Define

|                 | ID3   | ID2   | ID1  | ID0  |
|-----------------|-------|-------|------|------|
| JHT00(1100 )    | X     | X     | R361 | R357 |
| JHT01 (1101 )   | X     | X     | R361 | R355 |
| JHL90 (1110 )   | X     | X     | R360 | R357 |
| JHL91 (1111 )   | X     | X     | R360 | R355 |
| KHLB0 (0000 )   | R1052 | R1150 | R922 | R928 |
| KHLB1( 0001 )   | R1052 | R1150 | R922 | R923 |
| KHLB2( 0010 )   | R1052 | R1150 | R927 | R928 |
| 12 inch( 0011 ) | X     | X     | X    | X    |
| 12 inch( 0100 ) | X     | X     | X    | X    |
| 12 inch( 0101 ) | X     | X     | X    | X    |
| Reserve (0110 ) | X     | X     | X    | X    |
| Reserve (0111 ) | X     | X     | X    | X    |
| Reserve (1000 ) | X     | X     | X    | X    |
| Reserve (1001 ) | X     | X     | X    | X    |
| Reserve (1010 ) | X     | X     | X    | X    |
| Reserve (1011 ) | X     | X     | X    | X    |

## VGA and DDR2 Voltage Rails (NB9M-GS)

| State \ power plane            |   |   | +1.8VS | +3VS<br>+VGA_CORE<br>+1.1VS |
|--------------------------------|---|---|--------|-----------------------------|
| S0                             | ○ | ○ | ○      | ○                           |
| S1                             | ○ | ○ | ○      | ○                           |
| S3                             | ○ | ○ | ✗      | ✗                           |
| S5 S4/AC                       | ○ | ○ | ✗      | ✗                           |
| S5 S4/ Battery only            | ○ | ✗ | ✗      | ✗                           |
| S5 S4/AC & Battery don't exist | ✗ | ✗ | ✗      | ✗                           |

| GPIO   | I/O | ACTIVE | Function Description                               |
|--------|-----|--------|--|
| GPIO0  | N/A | N/A    | Available  |
| GPIO1  | IN  | -      | Hot plug detect for IFP link C                     |
| GPIO2  | OUT | H      | Panel Back-Light brightness(PWM)                   |
| GPIO3  | OUT | H      | Panel Power Enable                                 |
| GPIO4  | OUT | H      | Panel Back-Light On/Off (PWM)                      |
| GPIO5  | OUT | -      | GPU VID0   |
| GPIO6  | OUT | -      | GPU VID1   |
| GPIO7  | OUT | -      | GPU VID2 or MEM VID                                |
| GPIO8  | I/O | L      | Thermal Catastrophic Overtemp                      |
| GPIO9  | OUT | L      | FAN control and/or Thermal Alert (PWM)             |
| GPIO10 | OUT |        | Memory VREF switch                                 |
| GPIO11 | I/O | L      | SLI raster sync                                    |
| GPIO12 | IN  | -      | AC power detect pin                                |
| GPIO13 | OUT | -      | Power supply control                               |
| GPIO14 | OUT | -      | Power supply control                               |
| GPIO15 | IN  | -      | Hot plug detect for IFP link E                     |
| GPIO16 | IN  | -      | Dongle DVI Mode control for Primary Displayport    |
| GPIO17 | IN  | -      | Dongle HDMI Mode control for Primary Displayport   |
| GPIO18 | IN  | -      | Dongle DVI Mode control for Secondary Displayport  |
| GPIO19 | IN  | -      | Dongle HDMI Mode control for Secondary Displayport |
| GPIO20 | IN  | -      | Hot plug detect for IFP link D                     |
| GPIO21 | IN  | -      | Hot plug detect for IFP link E                     |
| GPIO22 | IN  | -      | SLI swap ready signal                              |
| GPIO23 | N/A | N/A    | Available  |

## VRAM POWER SEQUENCE

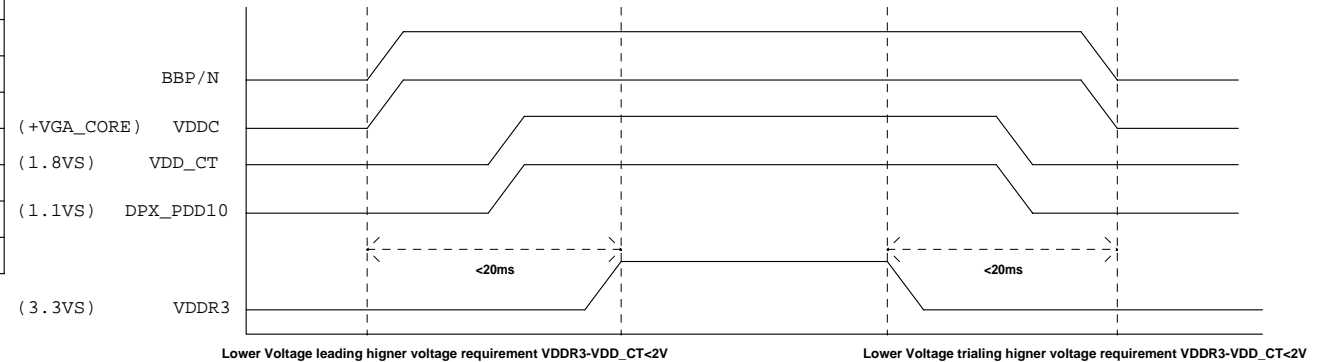
GDDR3 FOR 4 UNIT = 5.4A

## EDP at Tj = 97C\*

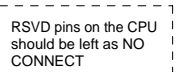
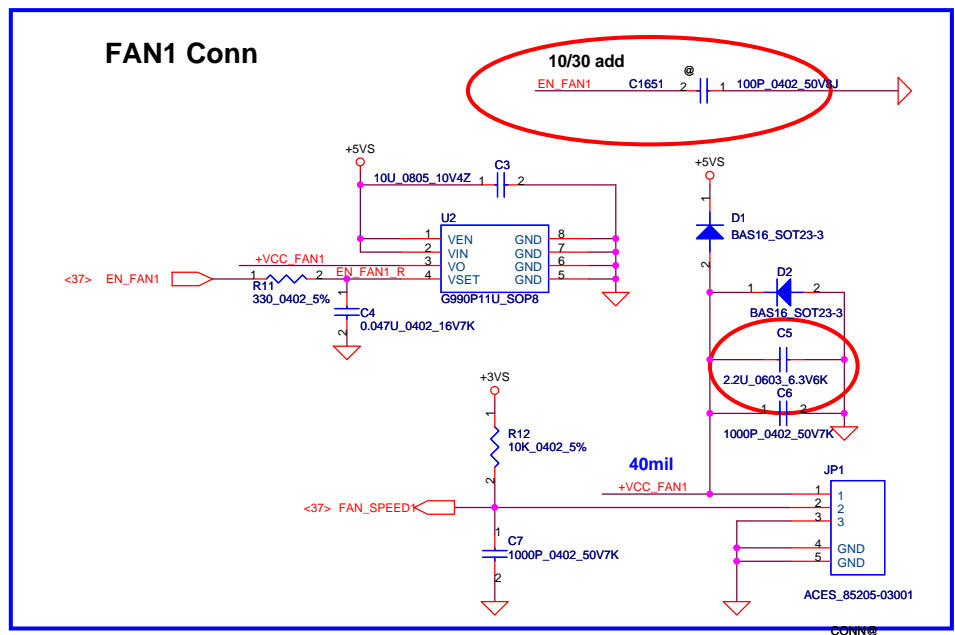
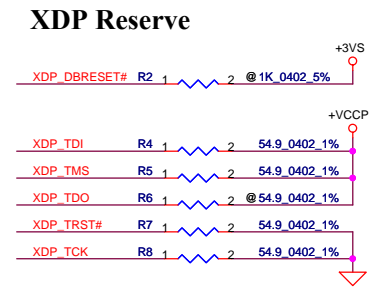
| Power Supply Rail |          | NB9P-GS |        | NB9P-GE2 |        |
|-------------------|----------|---------|--------|----------|--------|
| (V)               |          | GDDR3   | DDR2   | GDDR3    | DDR2   |
| NVVD              | Variable | 20.65A  | 16.96A | 18.47A   | 16.06A |
| FB_DLLAVDD        | 1.1      | 10mA    |        |          |        |
| FB_PLLAVDD        | 1.1      | 10mA    |        |          |        |
| IFPC_IOVDD        | 1.1      | 80mA    |        |          |        |
| IFPD_IOVDD        | 1.1      | 80mA    |        |          |        |
| IFPE_IOVDD        | 1.1      | 160mA   |        |          |        |
| IFPF_IOVDD        | 1.1      | 160mA   |        |          |        |
| PEX_IOVDD/Q       | 1.1      | 1550mA  |        |          |        |
| PEX_PLLVDD        | 1.1      | 90mA    |        |          |        |
| PLLVD             | 1.1      | 45mA    |        |          |        |
| SP_PLLVDD         | 1.1      | 45mA    |        |          |        |
| VID_PLLVDD        | 1.1      | 45mA    |        |          |        |
| TOTAL             | 1.1      | 2.3A    |        |          |        |
| FBVDD/Q           | 1.8      | 3.37A   | 2.02A  | 3.21A    | 2.25A  |
| IFPA_IOVDD        | 1.8      | 95mA    |        |          |        |
| IFPB_IOVDD        | 1.8      | 95mA    |        |          |        |
| IFPAB_PLLVDD      | 1.8      | 70mA    |        |          |        |
| IFPCD_PLLVDD      | 1.8      | 25mA    |        |          |        |
| IFPEF_PLLVDD      | 1.8      | 85mA    |        |          |        |
| TOTAL             | 1.8      | 5.76A   | 3.69A  | 5.47A    | 3.96A  |
| DACA_VDD          | 3.3      | 110mA   |        |          |        |
| DACB_VDD          | 3.3      | 120mA   |        |          |        |
| DACC_VDD          | 3.3      | 110mA   |        |          |        |
| MIOA_VDDQ         | 3.3      | 10mA    |        |          |        |
| MIOB_VDDQ         | 3.3      | 10mA    |        |          |        |
| VDD33             | 3.3      | 150mA   |        |          |        |
| TOTAL             | 3.3      | 0.51A   |        |          |        |

## POWER UP/DOWN Sequence

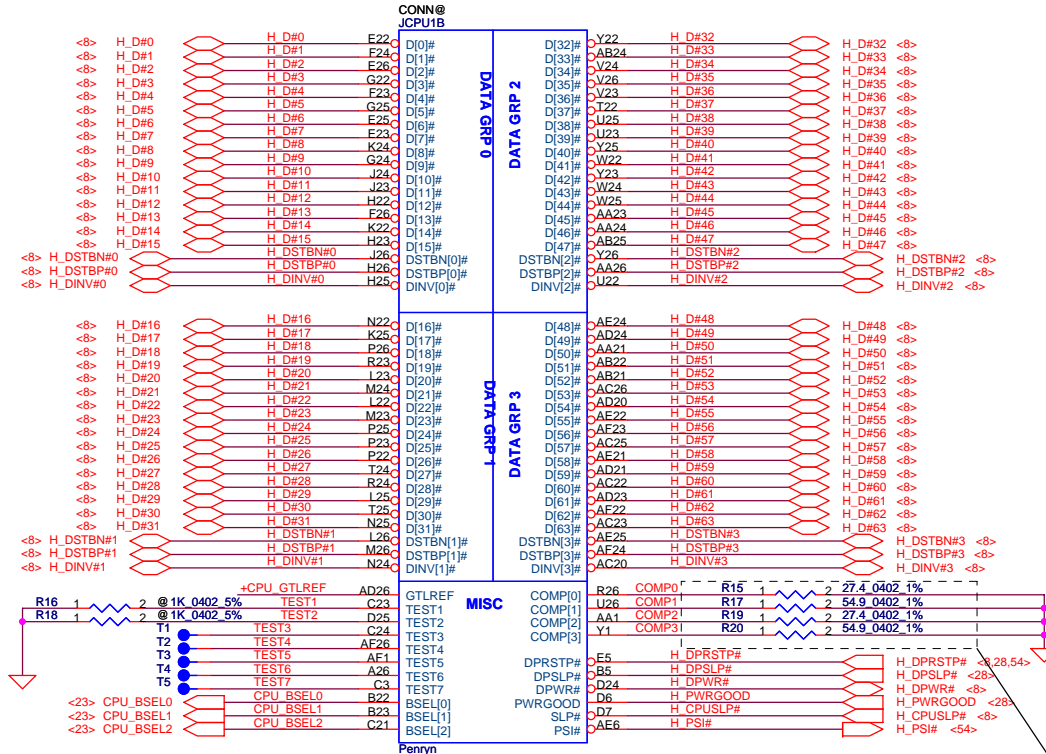
BBP must ramp up before or at the same time as VDDC but not after(ensure that BBP&gt;= VDDC at all times)



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|   |                    |                 |            | Date:                    | Monday, January 19, 2009 | Sheet 4 of 56 |



|   |                    |                 |            |                                |                    |     |
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|   |                    |                 |            | Custom                         | KHLBX MB Schematic | 1.0 |
|   |                    |                 |            | Date: Monday, January 19, 2009 | Sheet 5 of 56      |     |



Trace Close CPU < 0.5'

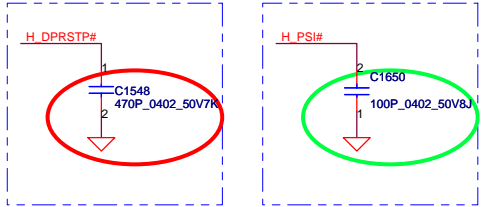
Width=4 mil ,  
Spacing: 15mil  
(550Ohm)

TRACE CLOSELY CPU < 0.5'

COMP0, COMP2 layout : Width 18mils and Space 25mils (27.4Ohms)  
COMP1, COMP3 layout : Width 5mils and Space 25mils (550Ohms)

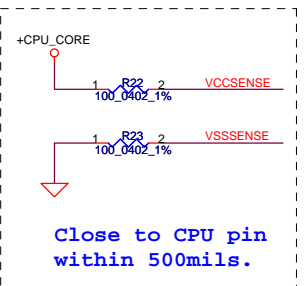
layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

| FSB  | BCLK | BSEL2 | BSEL1 | BSEL0 |
|------|------|-------|-------|-------|
| 533  | 133  | 0     | 0     | 1     |
| 667  | 166  | 0     | 1     | 1     |
| 800  | 200  | 0     | 1     | 0     |
| 1067 | 266  | 0     | 0     | 0     |



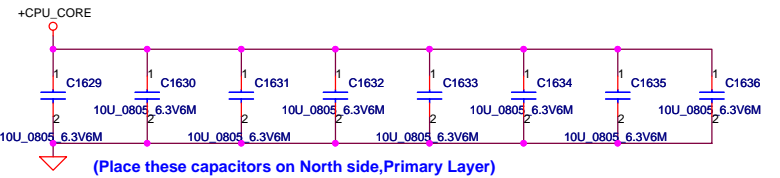
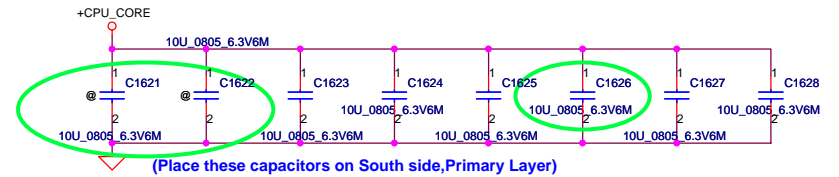
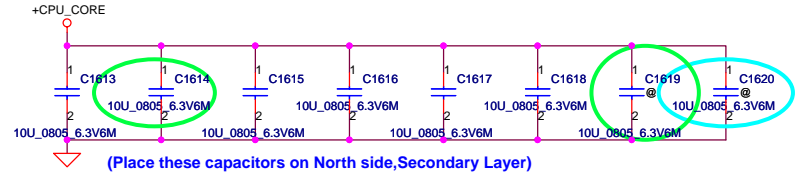
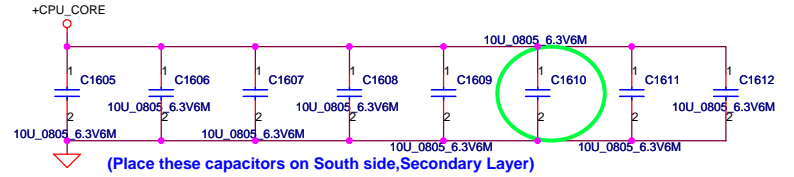
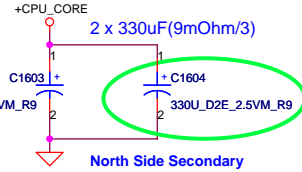
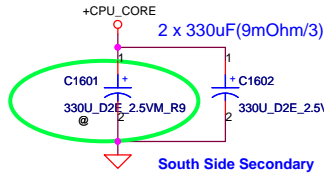
Length match within 25 mils.  
The trace width/space/other is 18/7/25.

Layout Note:  
Route VCCSENSE and VSSSENSE traces at 27.4 Ohms with 50 mil spacing.  
Place PU and PD within 1 inch of CPU.  
Length matched to within 25 mils.

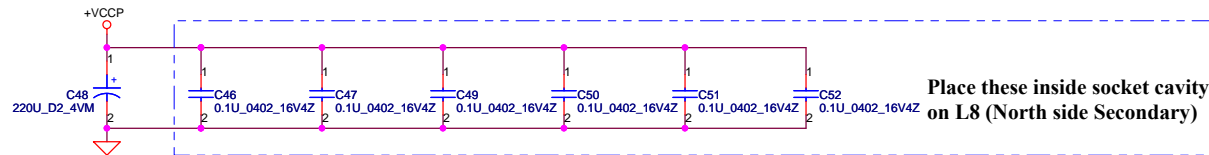


| CONN@JCPU1D |          |      |
|-------------|----------|------|
| A4          | VSS[001] | B6   |
| A8          | VSS[002] | P21  |
| A11         | VSS[003] | P24  |
| A14         | VSS[004] | R2   |
| A16         | VSS[005] | R5   |
| A19         | VSS[006] | R22  |
| A23         | VSS[007] | R25  |
| AF2         | VSS[008] | T1   |
| B6          | VSS[009] | T4   |
| B8          | VSS[010] | T23  |
| B11         | VSS[011] | T26  |
| B13         | VSS[012] | U3   |
| B16         | VSS[013] | U6   |
| B19         | VSS[014] | U21  |
| B21         | VSS[015] | U24  |
| B24         | VSS[016] | V2   |
| C5          | VSS[017] | V5   |
| C8          | VSS[018] | V22  |
| C11         | VSS[019] | V25  |
| C14         | VSS[020] | W1   |
| C16         | VSS[021] | W4   |
| C19         | VSS[022] | W23  |
| C2          | VSS[023] | W26  |
| C22         | VSS[024] | Y3   |
| C25         | VSS[025] | Y6   |
| D1          | VSS[026] | Y21  |
| D4          | VSS[027] | Y24  |
| D8          | VSS[028] | AA2  |
| D11         | VSS[029] | AA5  |
| D13         | VSS[030] | AA8  |
| D16         | VSS[031] | AA11 |
| D19         | VSS[032] | AA14 |
| D23         | VSS[033] | AA16 |
| D26         | VSS[034] | AA19 |
| E3          | VSS[035] | AA22 |
| E6          | VSS[036] | AA25 |
| E8          | VSS[037] | AB1  |
| E11         | VSS[038] | AB4  |
| E14         | VSS[039] | AB8  |
| E16         | VSS[040] | AB11 |
| E19         | VSS[041] | AB13 |
| E21         | VSS[042] | AB16 |
| E24         | VSS[043] | AB19 |
| F5          | VSS[044] | AB23 |
| F8          | VSS[045] | AB26 |
| F11         | VSS[046] | AC3  |
| F13         | VSS[047] | AC6  |
| F16         | VSS[048] | AC8  |
| F19         | VSS[049] | AC11 |
| F2          | VSS[050] | AC14 |
| F22         | VSS[051] | AC16 |
| F25         | VSS[052] | AC19 |
| G4          | VSS[053] | AC21 |
| G1          | VSS[054] | AC24 |
| G23         | VSS[055] | AD2  |
| G26         | VSS[056] | AD5  |
| H3          | VSS[057] | AD8  |
| H6          | VSS[058] | AD11 |
| H21         | VSS[059] | AD13 |
| H24         | VSS[060] | AD16 |
| J2          | VSS[061] | AD19 |
| J5          | VSS[062] | AD22 |
| J22         | VSS[063] | AD25 |
| J25         | VSS[064] | AE1  |
| K1          | VSS[065] | AE4  |
| K4          | VSS[066] | AE8  |
| K23         | VSS[067] | AE11 |
| K26         | VSS[068] | AE14 |
| L3          | VSS[069] | AE16 |
| L6          | VSS[070] | AE19 |
| L21         | VSS[071] | AE23 |
| L24         | VSS[072] | AE26 |
| M2          | VSS[073] | A2   |
| M5          | VSS[074] | AF6  |
| M22         | VSS[075] | AF8  |
| M25         | VSS[076] | AF11 |
| N1          | VSS[077] | AF13 |
| N4          | VSS[078] | AF16 |
| N23         | VSS[079] | AF19 |
| N26         | VSS[080] | AF21 |
| P3          | VSS[081] | A25  |
|             | VSS[163] | AF25 |

330u  
ESR 9m ohm  
Package (L\*W\*H) 7.3\*4.3\*1.8  
Rating 2.5V

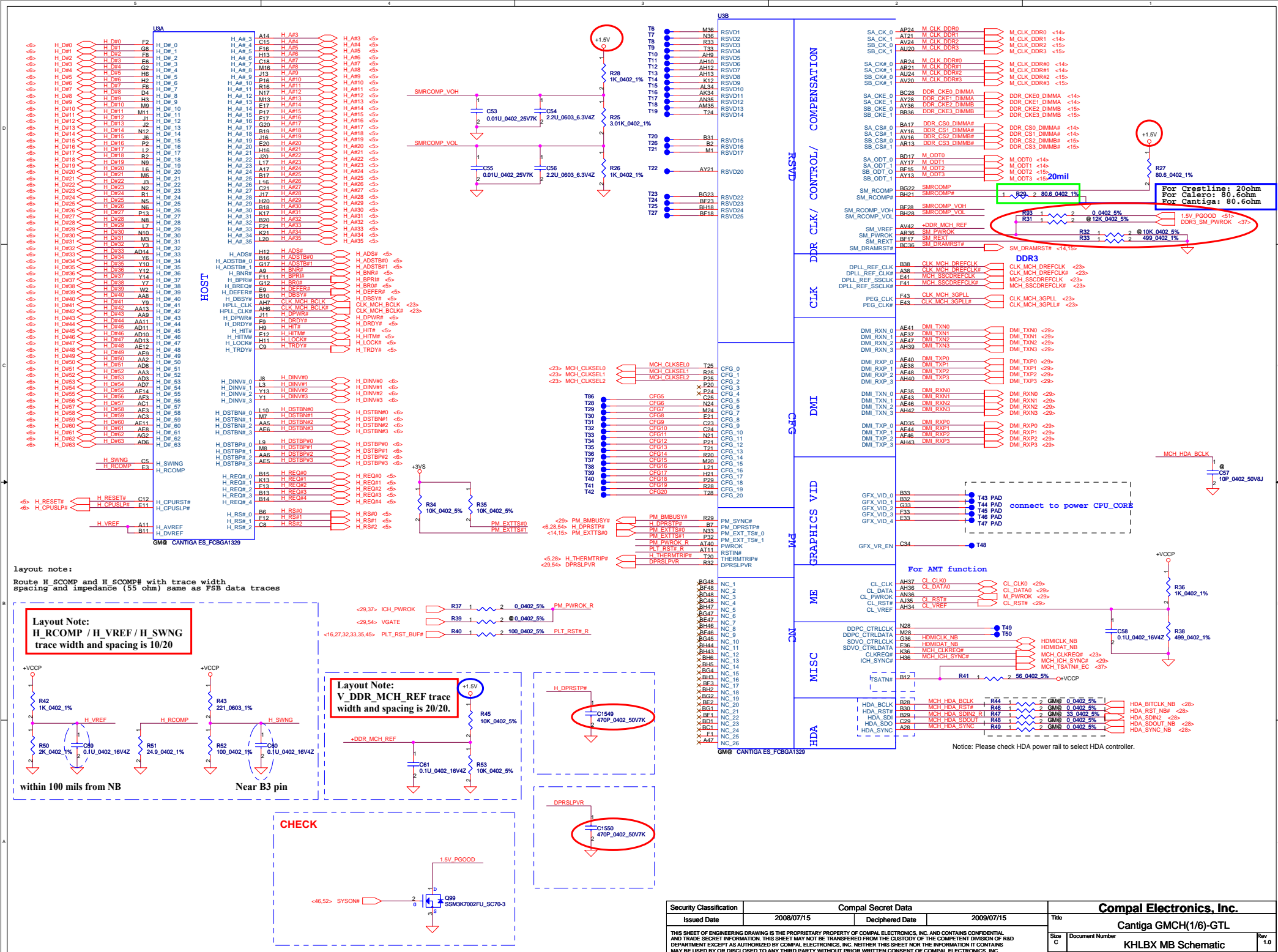


| +CPU-CORE<br>Decoupling | C,uF    | ESR, mohm | ESL,nH   |
|-------------------------|---------|-----------|----------|
| SPCAP, Polymer          | 6X330uF | 9m ohm/6  | 1.8nH/6  |
| MLCC 0805 X5R           | 32X22uF | 3m ohm/32 | 0.6nH/32 |
|                         | 32X10uF | 3m ohm/32 | 0.6nH/32 |



|   |  |                          |  |                 |  |                          |                 |                    |     |
|---|--|--------------------------|--|-----------------|--|--------------------------|-----------------|--------------------|-----|
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|   |  |                          |  |                 |  |                          |                 | Penryn (3/3)       |     |
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|   |  |                          |  |                 |  | B                        |                 | KHLBX MB Schematic | 1.0 |
|   |  |                          |  |                 |  |                          |                 |                    |     |
|   |  |                          |  |                 |  |                          |                 |                    |     |
| Date:   |  | Monday, January 19, 2009 |  |                 |  | Sheet                    |                 | 7 of 56            |     |





layout note:  
Route H\_SCOMP and H\_SCOMP# with trace width  
spacing and impedance (55 ohm) same as FSB data traces

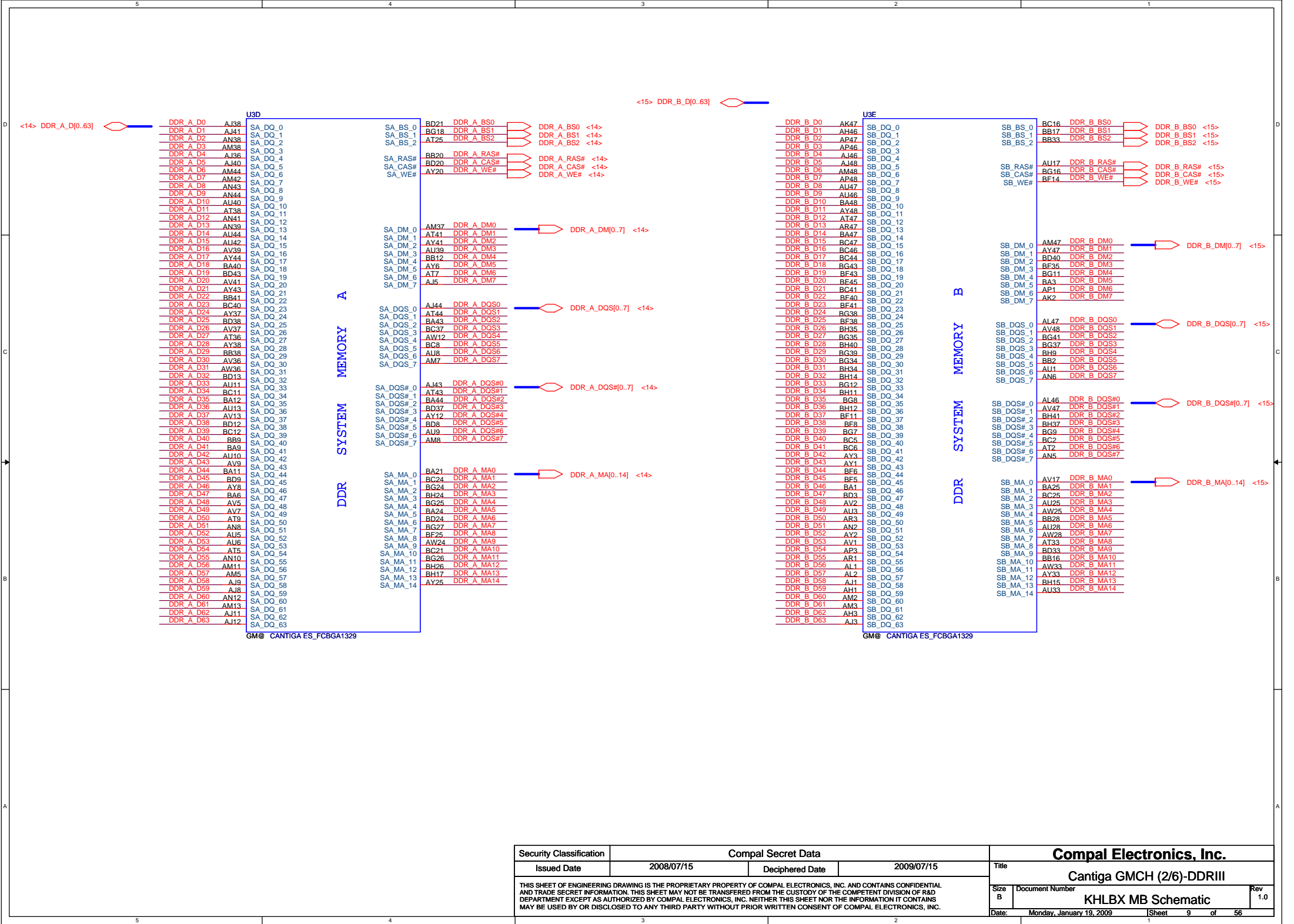
Layout Note:  
H\_RCOMP / H\_VREF / H\_SWNG  
trace width and spacing is 10/20

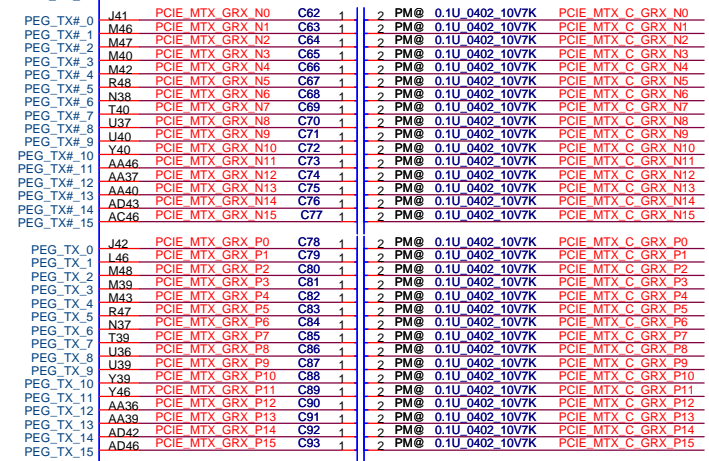
Layout Note:  
V\_DDR MCH REF trace  
width and spacing is 20/20.

CHECK

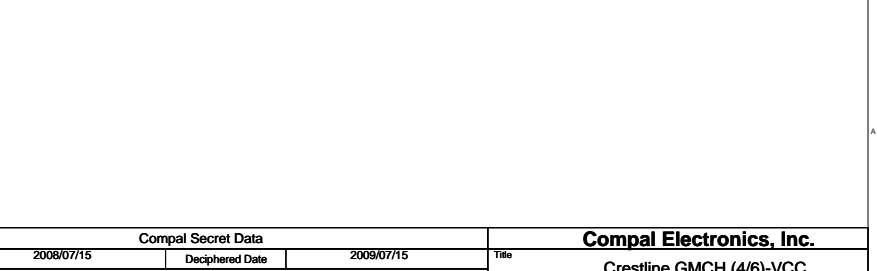
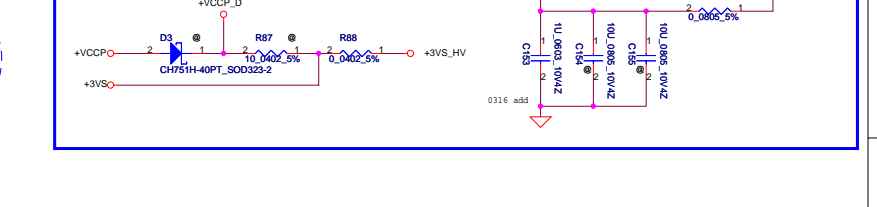
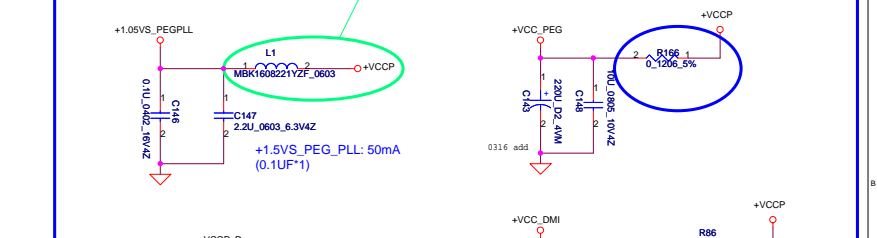
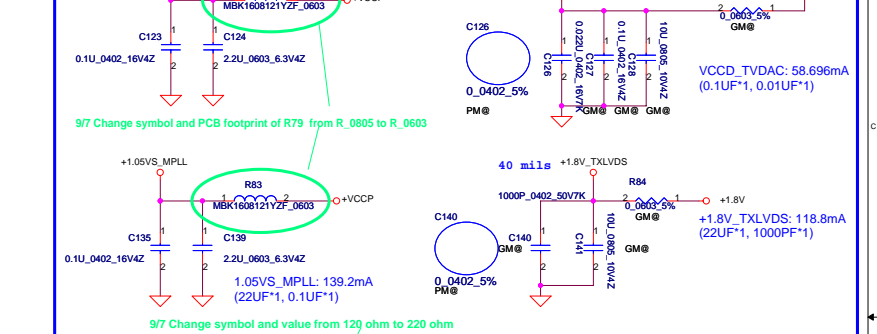
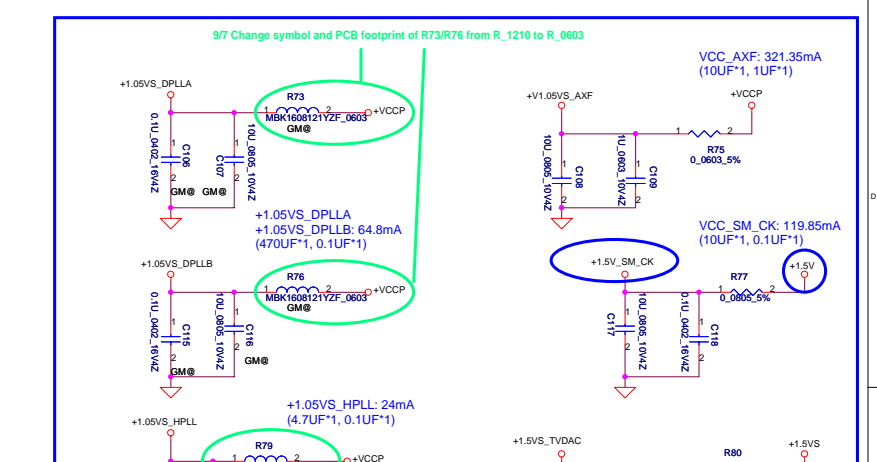
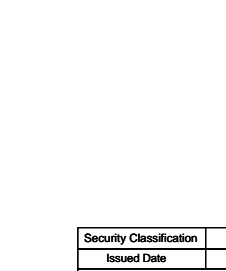
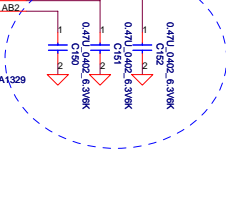
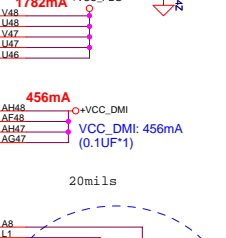
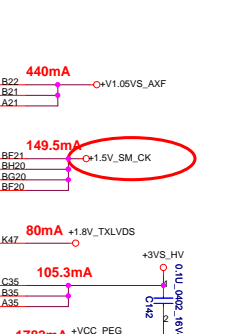
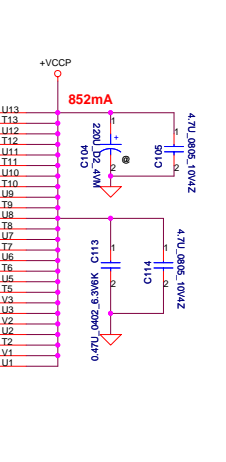
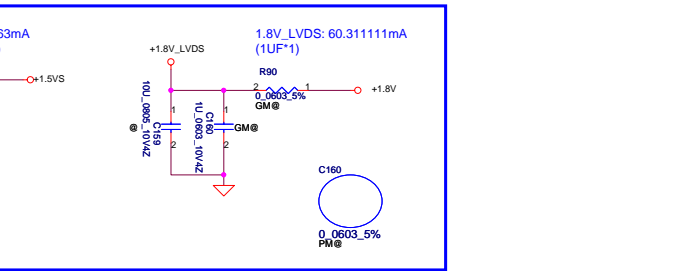
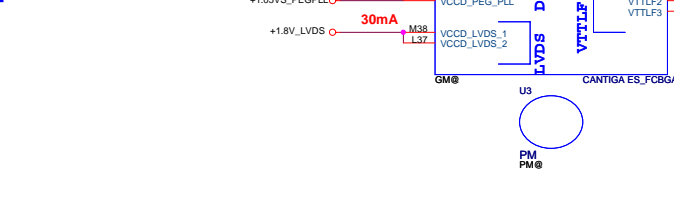
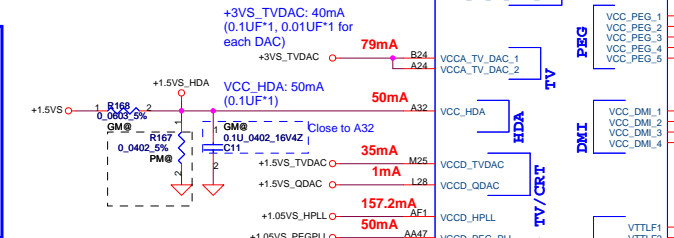
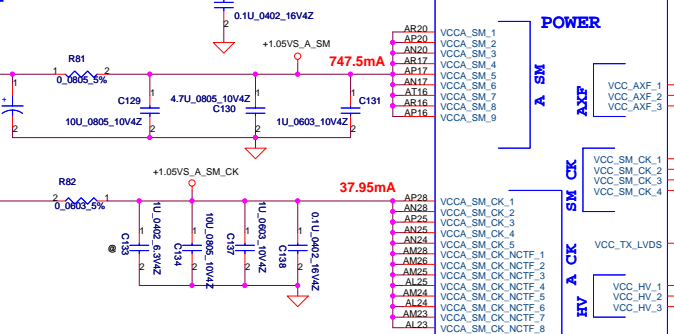
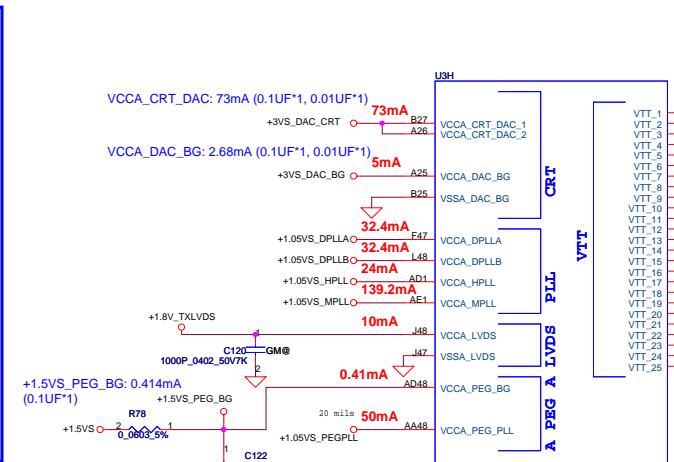
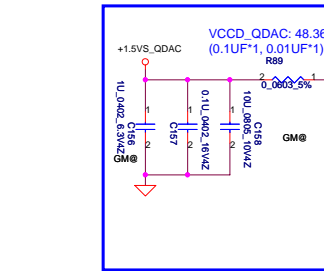
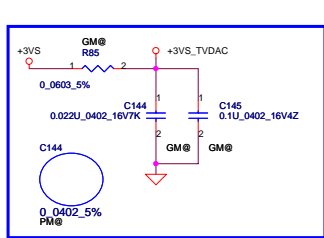
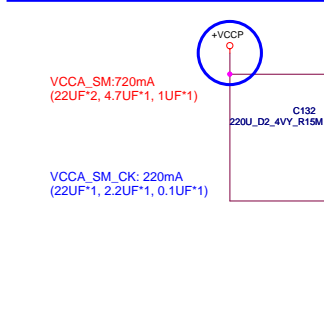
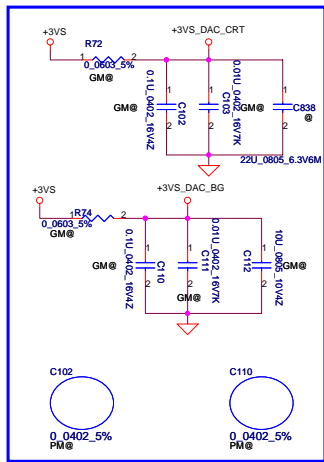
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| Security Classification   |  | Compal Secret Data |  | Title                    |  |
| Issued Date   |  | Deciphered Date    |  | Cantiga GMCH(1/6)-GTL    |  |
| 2008/07/15  |  | 2009/07/15         |  | KHLBX MB Schematic       |  |
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|   |  |                    |  | Sheet 8 of 56            |  |

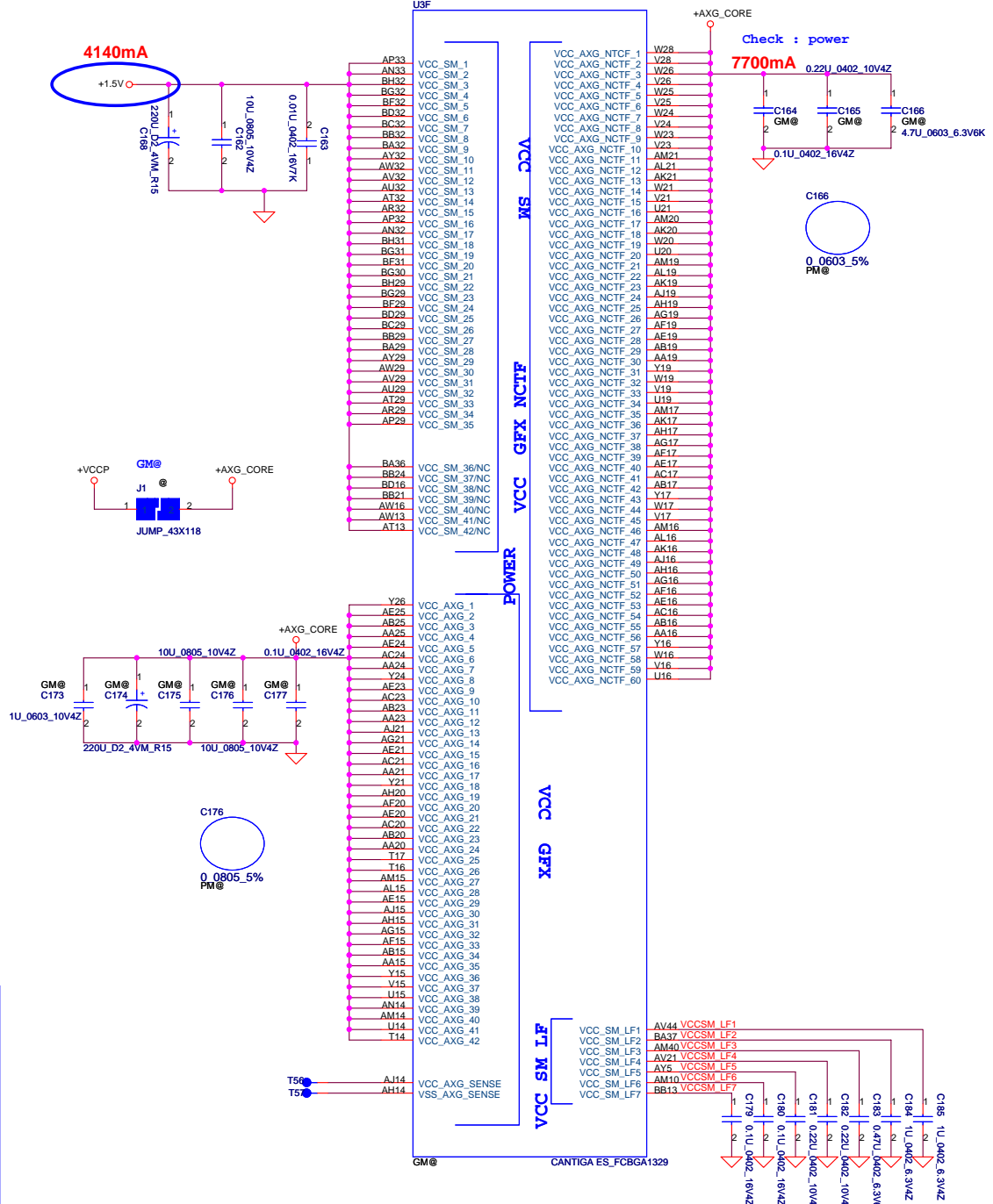






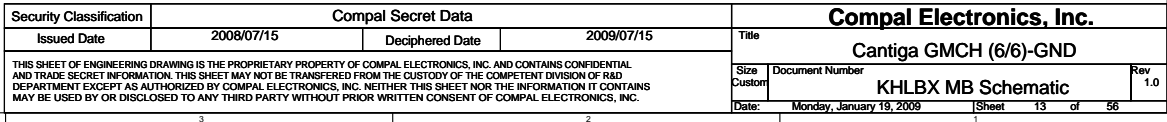
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|---|------------|--------------------|------------|-----------------------------------|--------------------|-----|
| Security Classification   |            | Compal Secret Data |            | Compal Electronics, Ltd.          |                    |     |
| Issued Date   | 2008/07/15 | Deciphered Date    | 2009/07/15 | Title<br>Cantiga(3/6)-VGA/LVDS/TV |                    |     |
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|   |            |                    |            | Custor                            | KHLBX MB Schematic | 1.0 |
|   |            |                    |            | Date: Monday, January 19, 2009    | Sheet 10 of 56     |     |





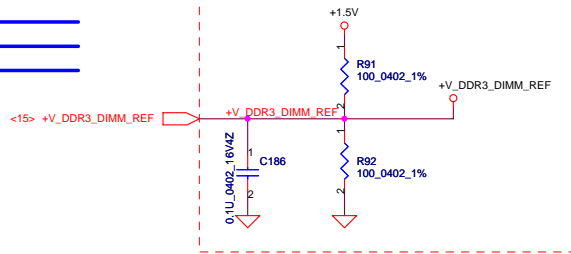
The diagram shows a circuit for a 500mV/div, 100ns/div oscilloscope probe. It starts with a +VCCP source connected to a 50 ohm resistor (C268). This is followed by a 50 ohm resistor (C269). The signal then passes through a series combination of a 10 pF capacitor (C270) and a 50 ohm resistor (C276). The signal then passes through a 10 pF capacitor (C339) and a 50 ohm resistor (C340) in parallel, which is connected to the oscilloscope input. The probe is connected to a +VCCP source and a ground symbol.

|   |            |                    |            |                                   |                                       |            |
|---|------------|--------------------|------------|-----------------------------------|---------------------------------------|------------|
| Security Classification   |            | Compal Secret Data |            | Compal Electronics, Inc.          |                                       |            |
| Issued Date   | 2008/07/15 | Deciphered Date    | 2009/07/15 | Title<br>Crestline GMCH (5/6)-VCC |                                       |            |
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|   |            |                    |            | Date: Monday, January 19, 2009    |                                       |            |
|   |            |                    |            | Sheet 12 of 56                    |                                       |            |



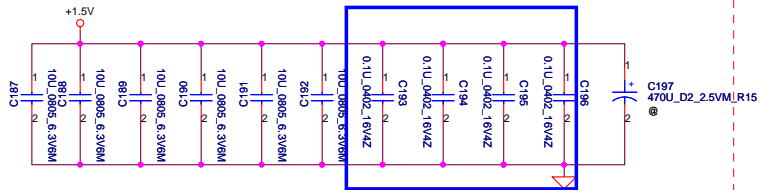


<9> DDR\_A\_DQS#[0..7]  
<9> DDR\_A\_D[0..63]  
<9> DDR\_A\_DM[0..7]  
<9> DDR\_A\_DQS[0..7]  
<9> DDR\_A\_MA[0..14]

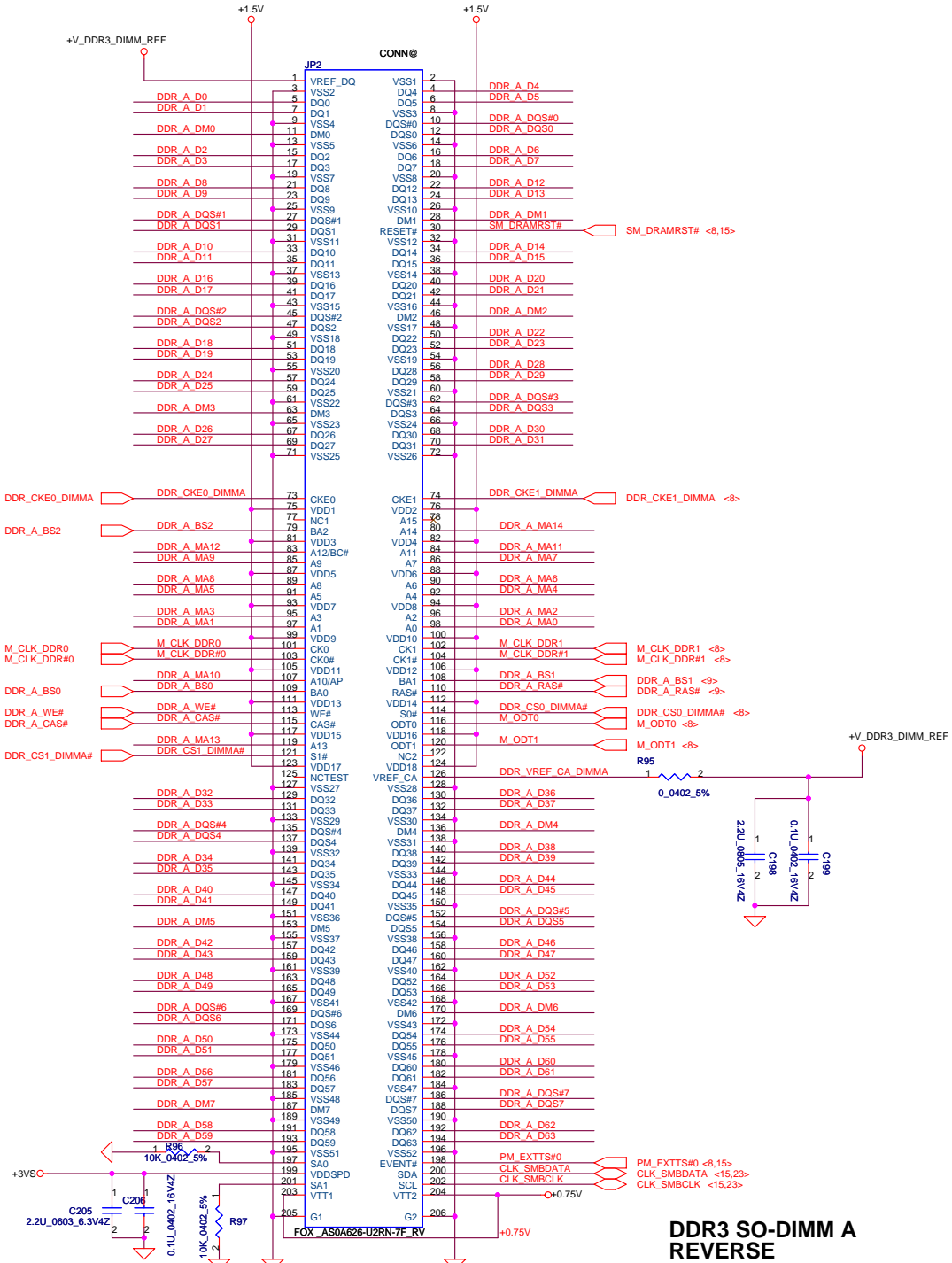
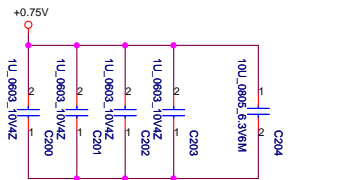


Layout Note:  
Place near JP4

Layout Note: Place these 4 Caps near Command  
and Control signals of DIMMA



Layout Note:  
Place near JP4.203 & JP4.204



## DDR3 SO-DIMM A REVERSE

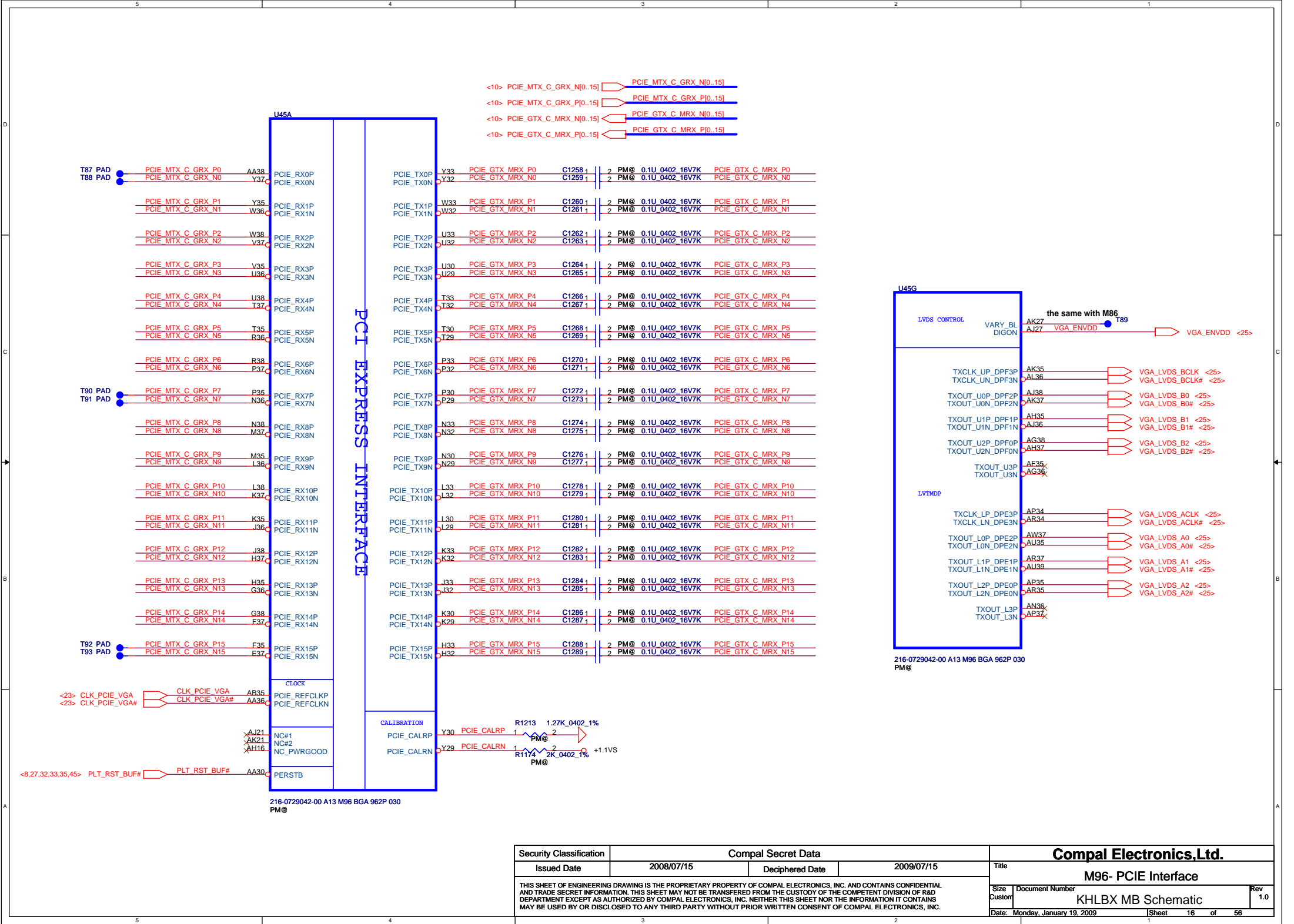
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| Issued Date   | 2008/07/15               | Deciphered Date    | 2009/07/15 | Title                    |  |
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| Size  | Document Number          | Rev                |            | KHLBX MB Schematic       |  |
| Date  | Monday, January 19, 2009 | Sheet              | 14         | of 56                    |  |



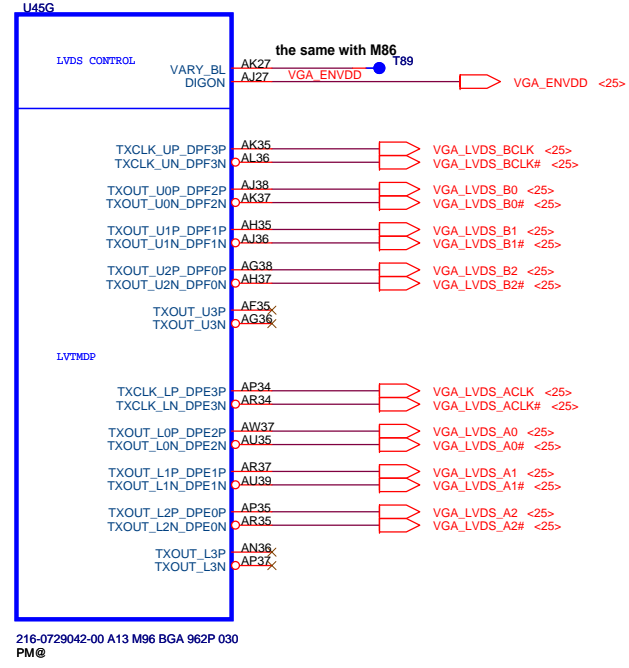
### DDR3 SO-DIMM B REVERSE

|  |            |                    |            |                                |                     |         |
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| Security Classification  |            | Compal Secret Data |            | Compal Electronics, Inc.       |                     |         |
| Issued Date  | 2008/07/15 | Deciphered Date    | 2009/07/15 | Title                          | DDRIII-SODIMM SLOT2 |         |
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|  |            |                    |            | KHLBX MB Schematic             |                     |         |
|  |            |                    |            | Date: Monday, January 19, 2009 | Sheet 15 of 56      |         |



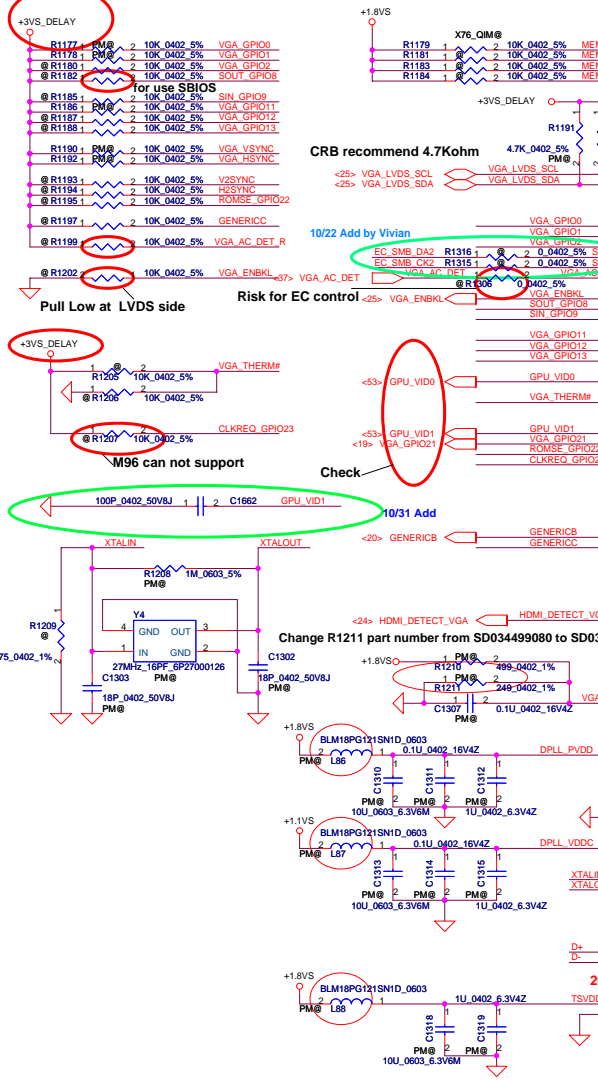


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<10> PCIE\_MTX\_C\_GRX\_P[0..15] PCIE\_MTX\_C\_GRX\_P[0..15]  
<10> PCIE\_GTX\_C\_MRX\_N[0..15] PCIE\_GTX\_C\_MRX\_N[0..15]  
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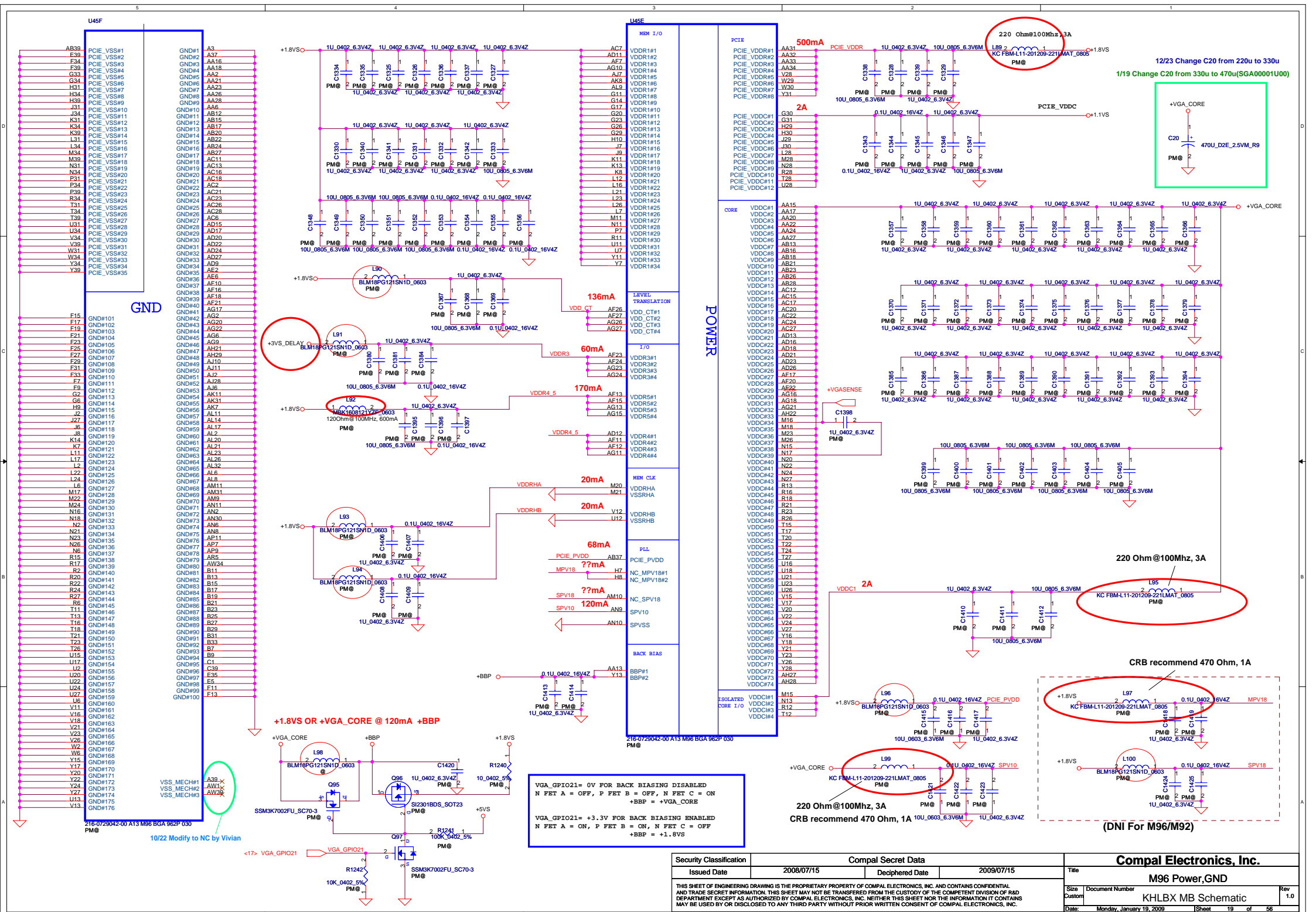


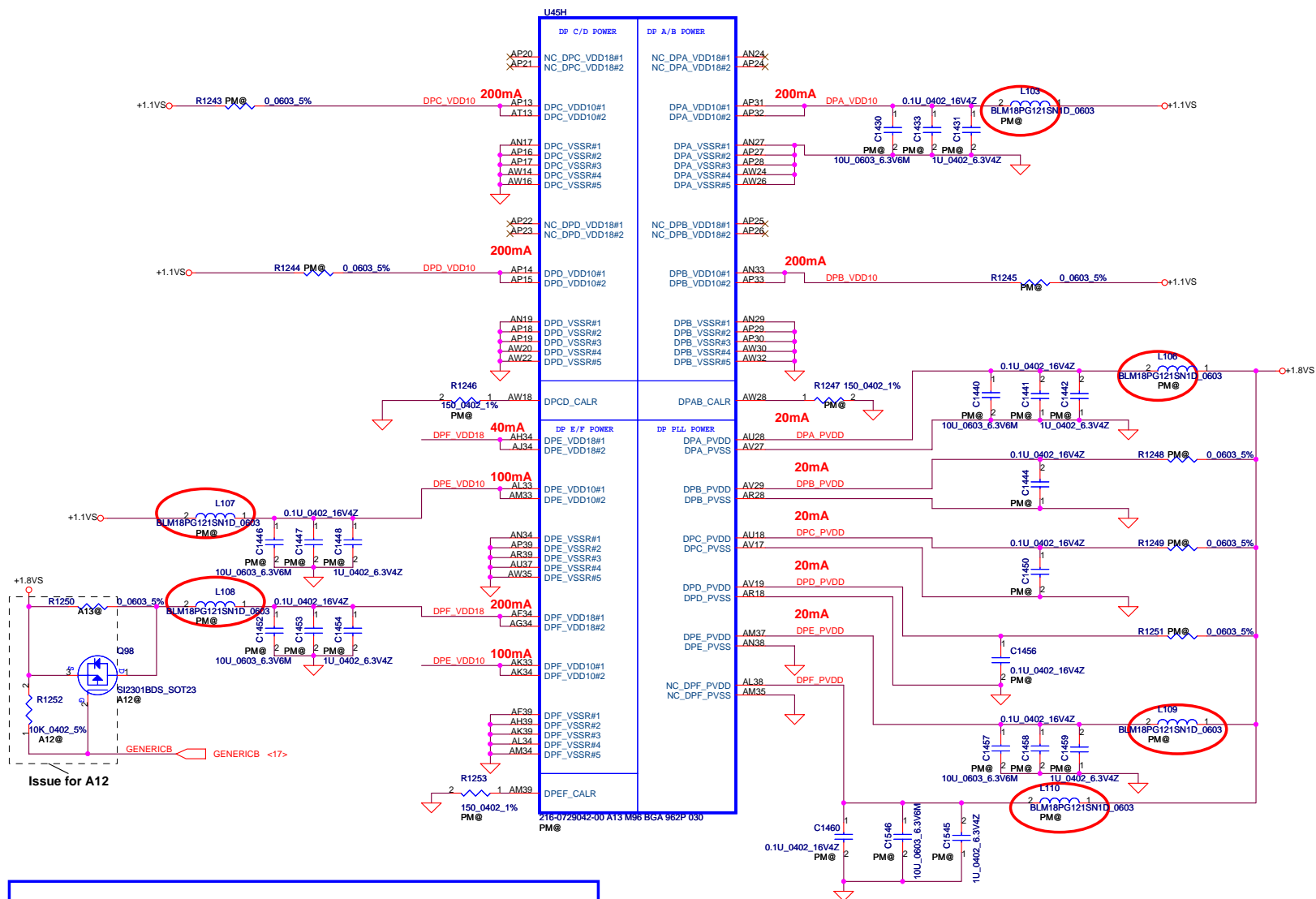
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| Security Classification   |  | Compal Secret Data |  |                 |  | Compal Electronics,Ltd. |  |                          |  |
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|   |  |                    |  |                 |  | Size                    |  | Document Number          |  |
|   |  |                    |  |                 |  | Custom                  |  | KHLBX MB Schematic       |  |
|   |  |                    |  |                 |  | Date:                   |  | Monday, January 19, 2009 |  |
|   |  |                    |  |                 |  | Sheet                   |  | 16 of 56                 |  |
|   |  |                    |  |                 |  | Rev                     |  | 1.0                      |  |

| Strap Name                          | Pin                        | Straps description   | Default Value |
|-------------------------------------|----------------------------|--|---------------|
| TX_PWRS_ENB                         | GPIO0                      | Transmitter Power Saving Enable<br>0: 50% Tx output swing for mobile mode<br>1: full Tx output swing (Default setting for Desktop)   | 1             |
| TX_DEEMPH_EN                        | GPIO1                      | PCI Express Transmitter De-emphasis Enable<br>0: Tx de-emphasis disabled for mobile mode<br>1: Tx de-emphasis enabled (Default setting for desktop)  | 1             |
| BIF_GEN2_EN                         | GPIO2                      | Advertises the PCI-E device as 2.5 GT/s capable at power-on<br>1= Advertises the PCI-E device as 5.0 GT/s capable at power-on<br>0: CLKREQ# Power Management   | 0             |
| STRAP_BIF_CLK_PM_EN                 | GPIO22                     | 0: CLKREQ# power management capability is disabled<br>1: CLKREQ# power management capability is enabled<br>GPIO13,12,11 (config 2,1,0):  | 0             |
| CONFIG[2]<br>CONFIG[1]<br>CONFIG[0] | GPIO13<br>GPIO12<br>GPIO11 | a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type.<br>b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size.<br>memory apertures<br>CONFIG[3:0]<br>128 MB 000<br>256 MB 001<br>64 MB 010   | 001           |
| BIOS_ROM_EN                         | GPIO22                     | Enable external BIOS ROM device<br>0: Disable, 1: Enable   | 0             |
| AUD[1]<br>AUD[0]                    | HSYNC<br>VSYNC             | 00: No audio function; 10: Audio for DisplayPort only;<br>01: Audio for DisplayPort and HDMI if adapter is detected;<br>11: Audio for both DisplayPort and HDMI  | 1             |
| CCBYPASS<br>SMS_EN_HARD             | GENERICC<br>H2SYNC         |  | 0             |
| VIP_DEVICE<br>STRAP_DIS             | V2SYNC                     | If VIP_DEVICE_STRAP_EN is set to ?? then this pin is used to sense whether a VIP slave device is connected to the VIP Host interface. If VIP_DEVICE_STRAP_EN is set to ?? then this pin is not used as a strap at all (i.e. its value during reset is unimportant), and it can be used as a regular GPIO | 0             |





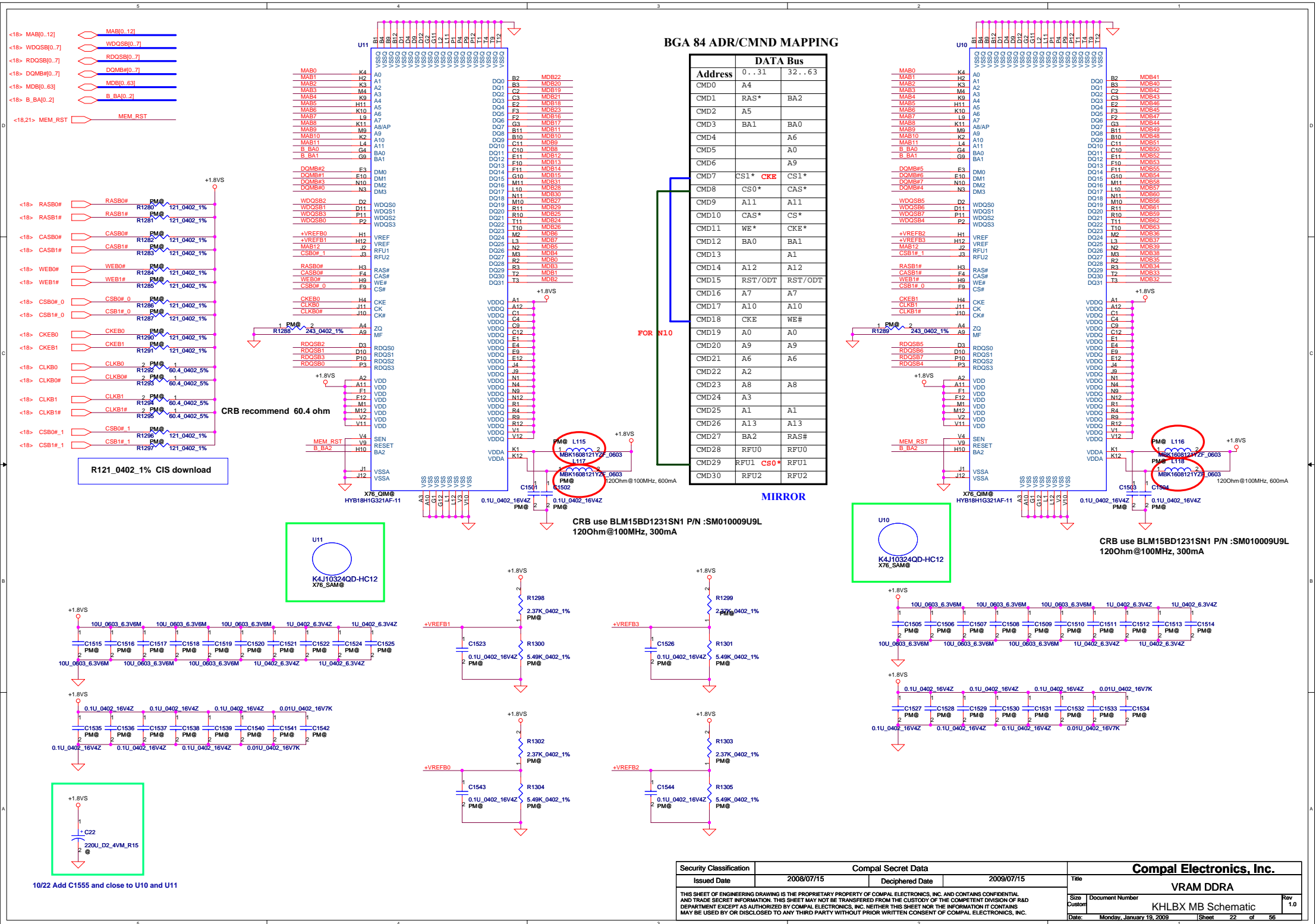




|   |  |                    |                 |                          |        |                          |  |       |     |    |    |
|---|--|--------------------|-----------------|--------------------------|--------|--------------------------|--|-------|-----|----|----|
| Security Classification   |  | Compal Secret Data |                 | Compal Electronics, Ltd. |        |                          |  |       |     |    |    |
| Issued Date   |  | 2008/07/15         | Deciphered Date | 2009/07/15               | Title  | M96                      |  |       |     |    |    |
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|   |  |                    |                 |                          | Custom | KHLBX MB Schematic       |  |       | 1.0 |    |    |
|   |  |                    |                 |                          | Date:  | Monday, January 19, 2009 |  | Sheet | 20  | of | 56 |
|   |  |                    |                 |                          |        |                          |  |       |     |    |    |

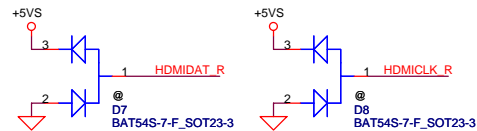




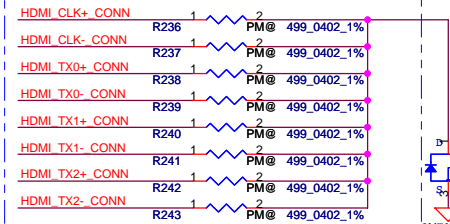




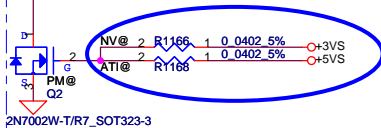




### TMDs pull down (500ohm) resistors G9x only

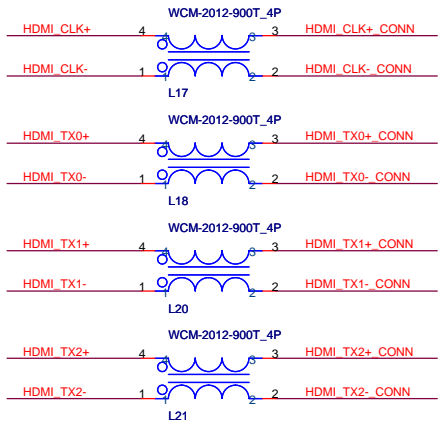


9/14 Modify for  
UMA used

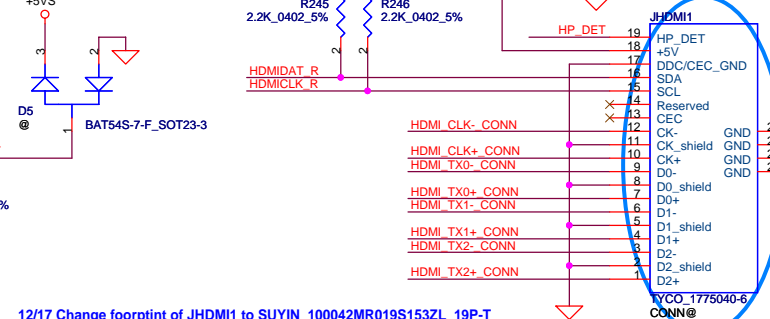
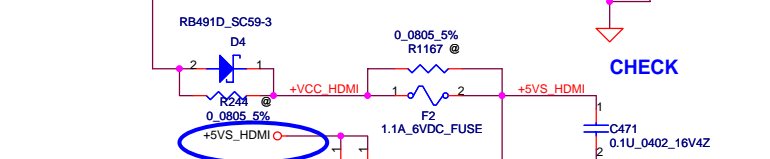
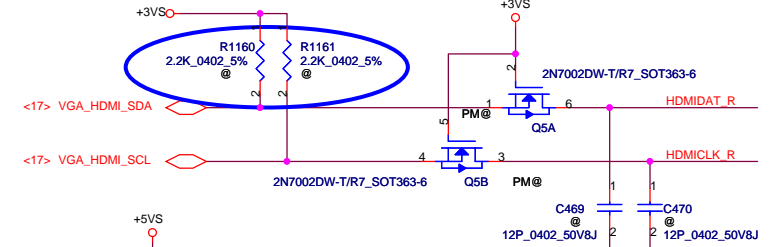
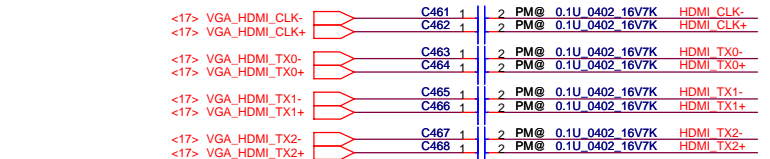


### NEAR CONNECT

9/14 Reserve for VGA  
used;check pin name



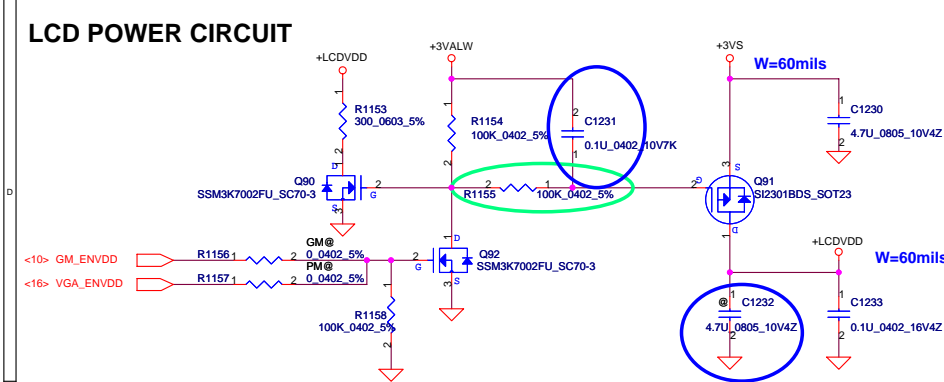
|           |      |   |           |                |
|-----------|------|---|-----------|----------------|
| HDMI CLK+ | R251 | 2 | 0.0402_5% | HDMI CLK+ CONN |
| HDMI CLK- | R252 | 2 | 0.0402_5% | HDMI CLK- CONN |
| HDMI TX0+ | R253 | 2 | 0.0402_5% | HDMI TX0+ CONN |
| HDMI TX0- | R254 | 2 | 0.0402_5% | HDMI TX0- CONN |
| HDMI TX1+ | R255 | 2 | 0.0402_5% | HDMI TX1+ CONN |
| HDMI TX1- | R256 | 2 | 0.0402_5% | HDMI TX1- CONN |
| HDMI TX2+ | R257 | 2 | 0.0402_5% | HDMI TX2+ CONN |
| HDMI TX2- | R258 | 2 | 0.0402_5% | HDMI TX2- CONN |



12/17 Change footprint of JHDMI1 to SUYIN\_100042MR019S153ZL\_19P-T

|   |  |  |  |                                |  |  |  |                         |  |  |  |
|---|--|--|--|--------------------------------|--|--|--|-------------------------|--|--|--|
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| Issued Date   |  |  |  | Deciphered Date                |  |  |  | Title                   |  |  |  |
| 2008/07/15  |  |  |  | 2009/07/15                     |  |  |  | Level Shifter_PS8101T   |  |  |  |
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|   |  |  |  | Custom                         |  |  |  | 1.0                     |  |  |  |
|   |  |  |  | Date: Monday, January 19, 2009 |  |  |  | Sheet 24 of 56          |  |  |  |

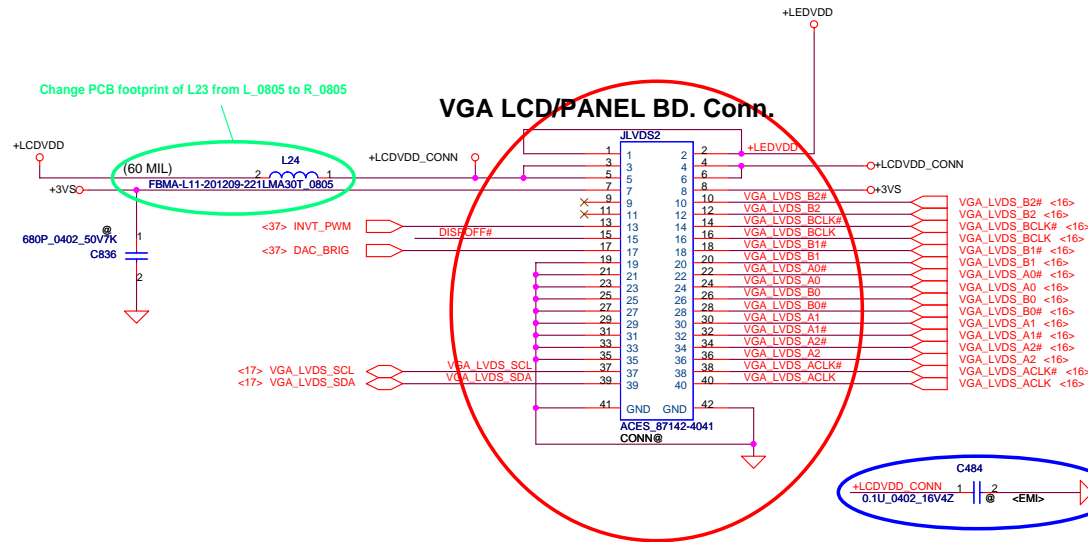
# LCD POWER CIRCUIT



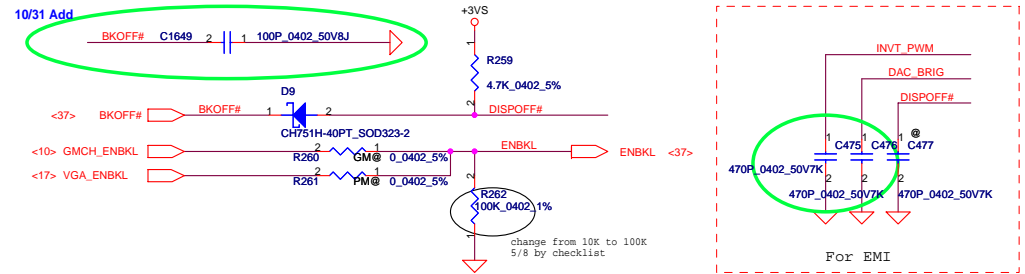
CHECK

Change PCB footprint of L22 from L\_0805 to R\_0805

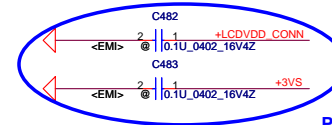
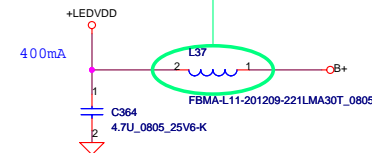
## VGA LCD/PANEL BD. Conn.



Place C484 close to JLVS2



Change PCB footprint of L37 from L\_0805 to R\_0805



Place C483 and C482 close to JLVS3

|   |  |                          |  |                 |  |                          |  |                      |  |         |
|---|--|--------------------------|--|-----------------|--|--------------------------|--|----------------------|--|---------|
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| Issued Date   |  | 2008/07/15               |  | Deciphered Date |  | 2009/07/15               |  | Title                |  |         |
|   |  |                          |  |                 |  |                          |  | LVDS & DVI Connector |  |         |
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| Size B  |  | Document Number          |  |                 |  | KHLBX MB Schematic       |  |                      |  | Rev 1.0 |
| Date:   |  | Monday, January 19, 2009 |  |                 |  | Sheet                    |  | 25 of 56             |  |         |

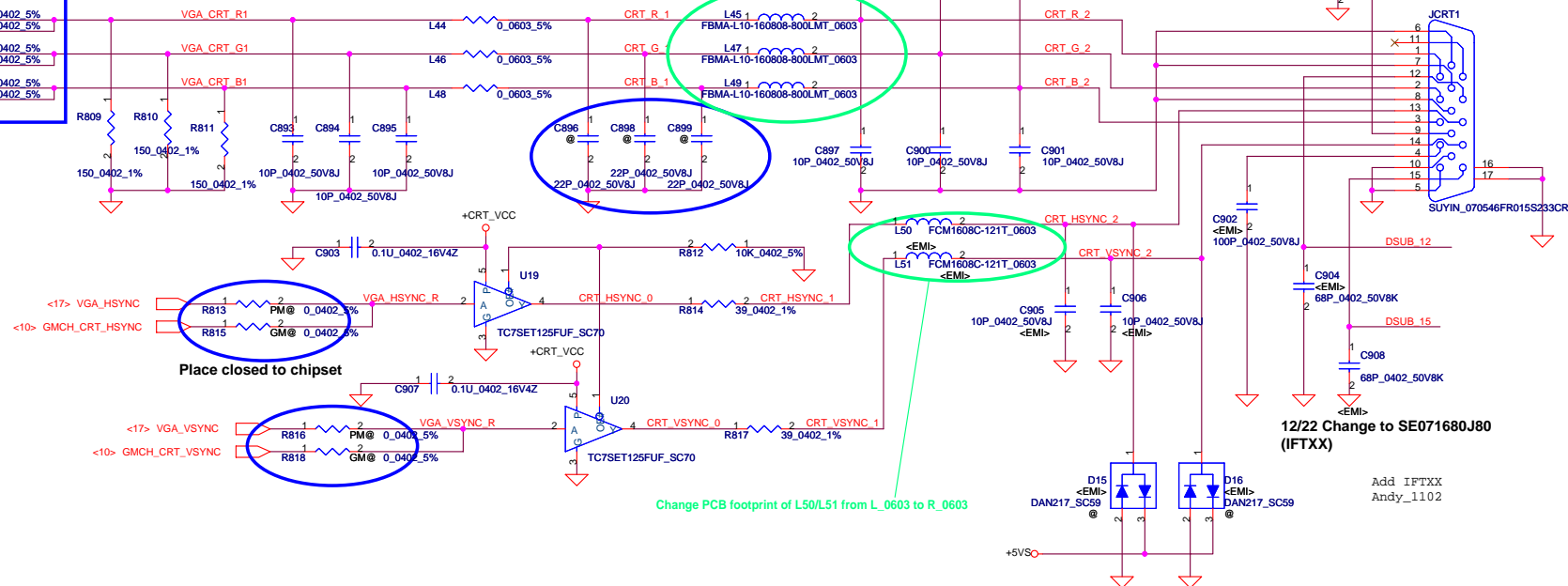
# CRT Connector

Checklist recommend: 2-pole filter on R/G/B signals  
C - L - C - L - C  
10p - 47 Ohm/100MHz - 22p - 47 Ohm/100MHz - 10p

12/15 Modified. Note L26~L30 are 0 Ohm resistors (IFTXX)

Place closed to chipset

|                 |      |   |   |               |
|-----------------|------|---|---|---------------|
| <17> VGA_CRT_R  | R803 | 1 | 2 | PM@ 0.0402 5% |
| <10> GMCH_CRT_R | R804 | 1 | 2 | GM@ 0.0402 5% |
| <17> VGA_CRT_G  | R805 | 1 | 2 | PM@ 0.0402 5% |
| <10> GMCH_CRT_G | R806 | 1 | 2 | GM@ 0.0402 5% |
| <17> VGA_CRT_B  | R807 | 1 | 2 | PM@ 0.0402 5% |
| <10> GMCH_CRT_B | R808 | 1 | 2 | GM@ 0.0402 5% |

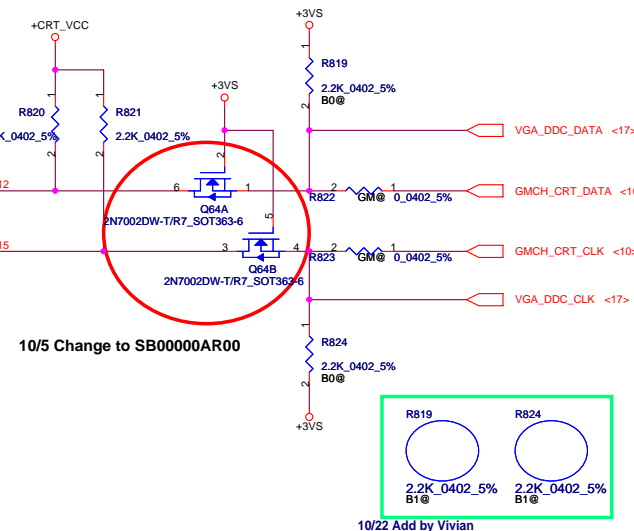


<17> VGA\_HSYNC  
<10> GMCH\_CRT\_HSYNC

Place closed to chipset

<17> VGA\_VSYNC  
<10> GMCH\_CRT\_VSYNC

Change PCB footprint of L50/L51 from L\_0603 to R\_0603

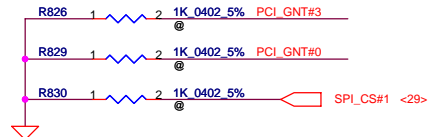
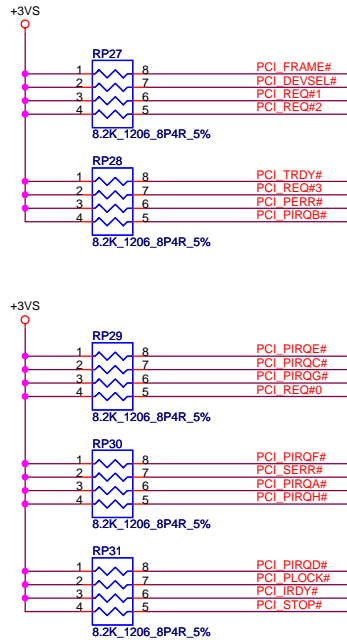


|   |  |                    |  |                 |  |                          |  |               |                 |                          |  |                    |    |    |         |
|---|--|--------------------|--|-----------------|--|--------------------------|--|---------------|-----------------|--------------------------|--|--------------------|----|----|---------|
| Security Classification   |  | Compal Secret Data |  |                 |  | Compal Electronics, Inc. |  |               |                 |                          |  |                    |    |    |         |
| Issued Date   |  | 2008/07/15         |  | Deciphered Date |  | 2009/07/15               |  | Title         |                 |                          |  |                    |    |    |         |
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|   |  |                    |  |                 |  |                          |  | Size B        | Document Number |                          |  | KHLBX MB Schematic |    |    | Rev 1.0 |
|   |  |                    |  |                 |  |                          |  | Date:         |                 | Monday, January 19, 2009 |  | Sheet              | 26 | of | 56      |

Compal Electronics, Inc.

CRT Connector

KHLBX MB Schematic

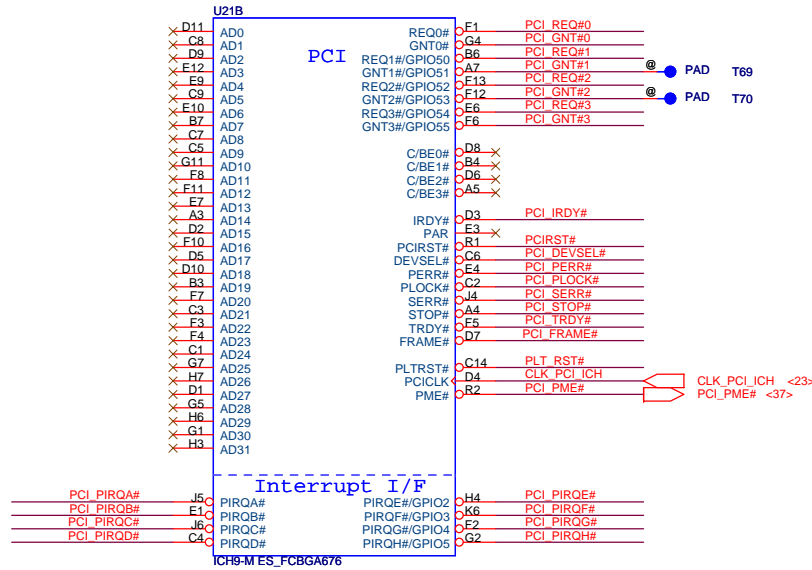


| A16 Swap Override Strap |   |
|-------------------------|---|
| PCI_GNT#3               | Low= A16 swap override Enable<br>High= Default* |

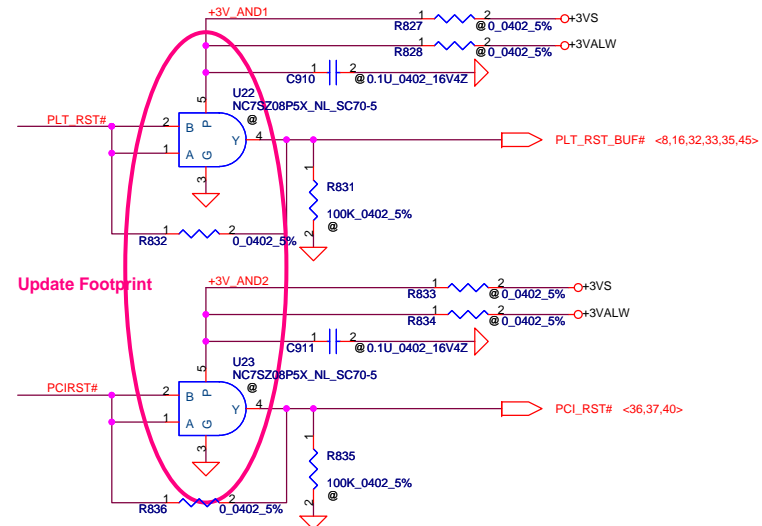
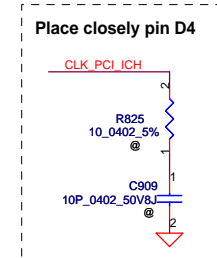
CRB: GNT#0 and SPI\_CS#1 have a weak internal pull up

| Boot BIOS Strap |          |                    |
|-----------------|----------|--------------------|
| PCI_GNT#0       | SPI_CS#1 | Boot BIOS Loaction |
| 0               | 1        | SPI                |
| 1               | 0        | PCI                |
| 1               | 1        | LPC*               |

9/18 Change U21 from SA00002JH00 to SA00002JH80

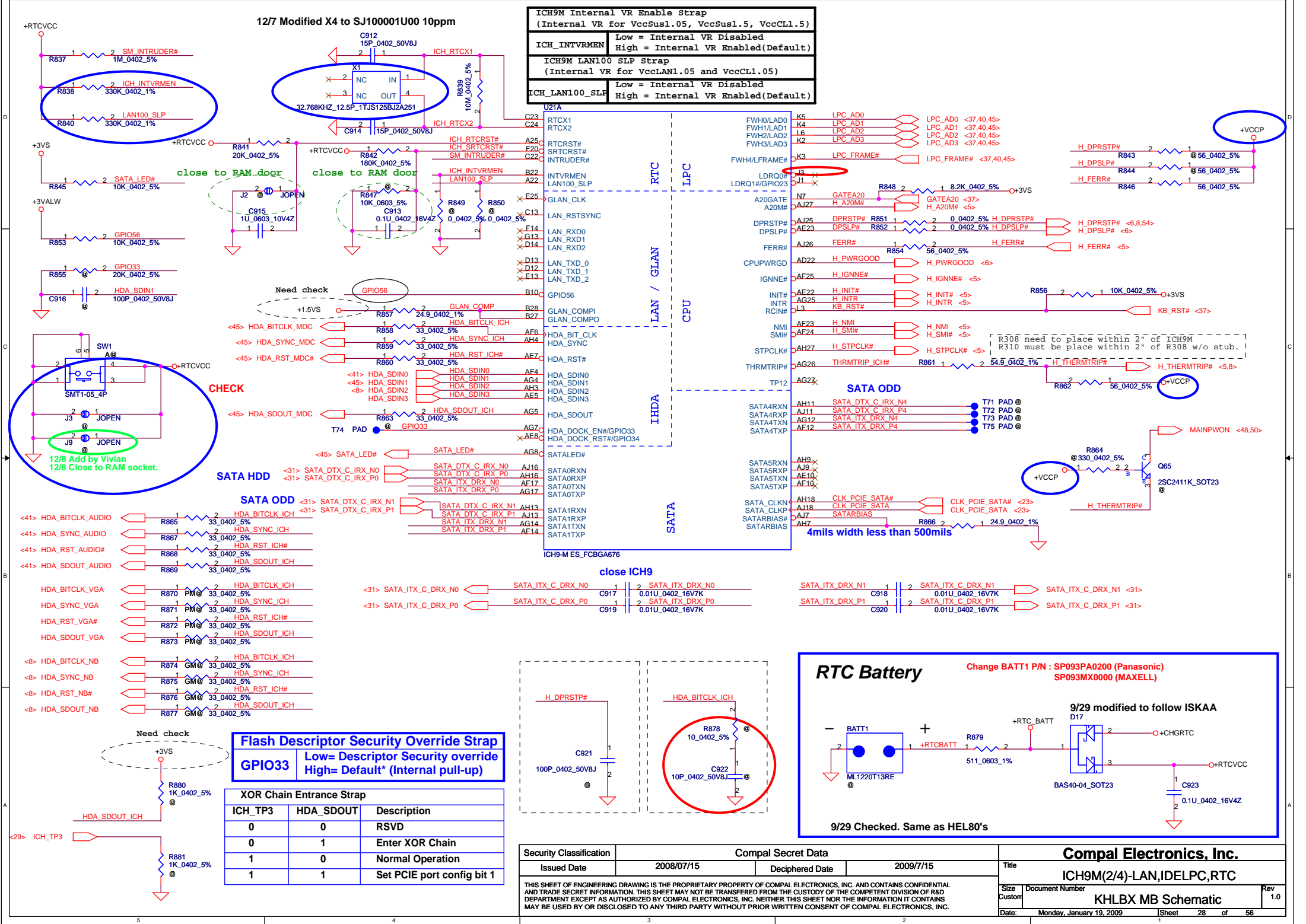


| DMI for ESI-compatible operation |  |
|----------------------------------|--|
| PCI_GNT#1                        | Low= DMI for ESI-compatible operation<br>High= Default* (Internal pull-up) |



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|-------------------------|--|------------|--|--------------------|--|------------|--------------------------|--------------------------------|--|
| Issued Date             |  | 2008/07/15 |  | Deciphered Date    |  | 2009/07/15 |                          | Title                          |  |
|                         |  |            |  |                    |  |            |                          | ICH9M(1/4)-PCI                 |  |
|                         |  |            |  |                    |  |            |                          | KHLBX MB Schematic             |  |
|                         |  |            |  |                    |  |            |                          | Rev 1.0                        |  |
|                         |  |            |  |                    |  |            |                          | Date: Monday, January 19, 2009 |  |
|                         |  |            |  |                    |  |            |                          | Sheet 27 of 56                 |  |

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**12/7 Modified X4 to SJ100001U00 10ppm**

**ICH9M Internal VR Enable Strap**  
(Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)  
Low = Internal VR Disabled  
High = Internal VR Enabled(Default)

**ICH9M LAN100 SLP Strap**  
(Internal VR for VccLAN1.05 and VccCL1.05)  
Low = Internal VR Disabled  
High = Internal VR Enabled(Default)

**U21A**  
FWH0/LAD0 K5 LPC\_AD0 LPC\_AD0 <37,40,45>  
FWH1/LAD1 K6 LPC\_AD1 LPC\_AD1 <37,40,45>  
FWH2/LAD2 K7 LPC\_AD2 LPC\_AD2 <37,40,45>  
FWH3/LAD3 K8 LPC\_AD3 LPC\_AD3 <37,40,45>  
FWH4/LFRAME# K3 LPC\_FRAME# LPC\_FRAME# <37,40,45>  
LDROQ# J1 X  
LDROQ1#/GPIO23 J1 X  
A20GATE A20M# N7 GATEA20 H\_A20M# 8.2K 0402 5% +3VS  
DPRSTP# AJ25 DPRSTP# R851 1 2 0 0402 5% H DPRSTP# H DPRSTP# <6,8,54>  
DPSLP# AE23 DPSLP# R852 1 2 0 0402 5% H DPSLP# H DPSLP# <6>  
FERR# AJ26 FERR# R854 1 2 56 0402 5% H\_FERR# H\_FERR# <5>  
CPUPWRGD AD22 H\_PWRGOOD H\_PWRGOOD <6>  
IGNNE# AE25 H\_IGNNE# H\_IGNNE# <5>  
INIT# AE22 H\_INIT# H\_INIT# <5>  
INTR RCIN# AG25 H\_INTR H\_INTR <5>  
KB\_RST# L3 KB\_RST# <37>  
NMI SM# AF23 H\_NMI# H\_NMI# <5>  
SMI# AF24 H\_SMI# H\_SMI# <5>  
STPCLK# AH27 H\_STPCLK# H\_STPCLK# <5>  
THRMTrip# AG26 THRMTrip ICH# R861 1 2 54.9 0402 1% H\_THERMTrip# H\_THERMTrip# <5,8>  
TP12 AG27 X

**SATA ODD**  
AH11 SATA DTX C\_IRX\_N4 T71 PAD @  
AJ11 SATA DTX C\_IRX\_P4 T72 PAD @  
AG12 SATA ITX DRX\_N4 T73 PAD @  
AF12 SATA ITX DRX\_P4 T75 PAD @  
SATA4RXN  
SATA4RXP  
SATA4TXN  
SATA4TXP  
SATA5RXN  
SATA5RXP  
SATA5TXN  
SATA5TXP  
SATA\_CLKN AH18 CLK\_PCIE\_SATA# CLK\_PCIE\_SATA# <23>  
SATA\_CLKP AJ18 CLK\_PCIE\_SATA CLK\_PCIE\_SATA <23>  
SATA\_BIAS AH7 X  
SATA\_BIAS R866 2 1 24.9 0402 1%  
4mils width less than 500mils

**Flash Descriptor Security Override Strap**  
GPIO33 Low= Descriptor Security override  
High= Default\* (Internal pull-up)

**XOR Chain Entrance Strap**

| ICH_TP3 | HDA_SDOOUT | Description                |
|---------|------------|----------------------------|
| 0       | 0          | RSVD                       |
| 0       | 1          | Enter XOR Chain            |
| 1       | 0          | Normal Operation           |
| 1       | 1          | Set PCIE port config bit 1 |

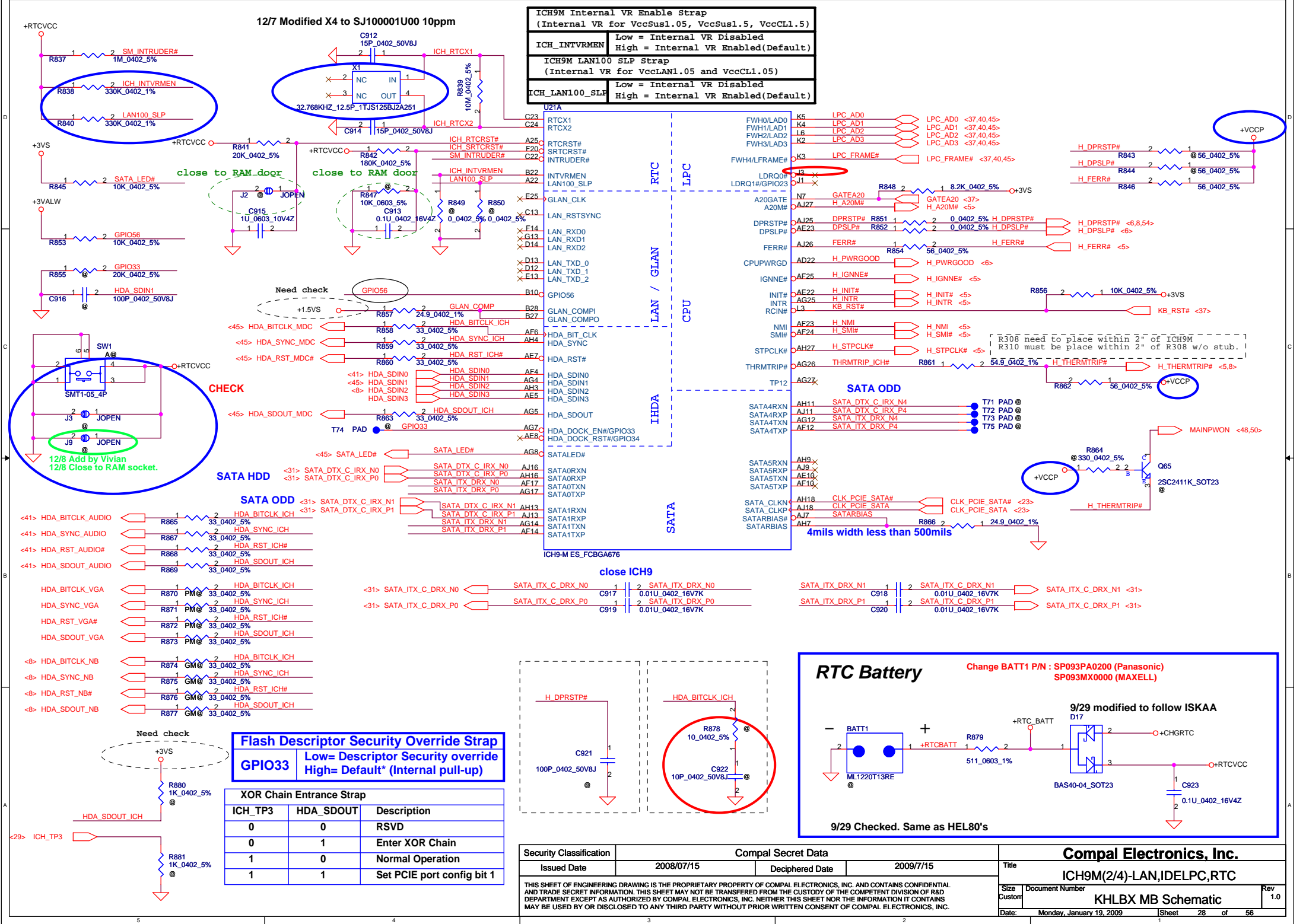
**RTC Battery**  
Change BATT1 P/N : SP093PA0200 (Panasonic)  
SP093MX0000 (MAXELL)

**9/29 modified to follow ISKAA**  
D17  
BATT1 ML1220T13RE  
+RTC BATT  
R879 511 0603 1%  
BAS40-04\_SOT23  
C923 0.1U 0402 16V4Z  
+RTC VCC

**9/29 Checked. Same as HEL80's**

**Compal Secret Data**  
Security Classification  
Issued Date 2008/07/15  
Deciphered Date 2009/7/15  
Title ICH9M(2/4)-LAN, IDELPC, RTC  
Size Custom  
Document Number KHLBX MB Schematic  
Date Monday, January 19, 2009  
Sheet 28 of 56

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12/7 Modified X4 to SJ100001U00 10ppm

IC9M Internal VR Enable Strap  
(Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)

ICH\_INTVRMEN Low = Internal VR Disabled  
High = Internal VR Enabled(Default)

ICH9M LAN100 SLP Strap  
(Internal VR for VccLAN1.05 and VccCL1.05)

ICH\_LAN100\_SLP Low = Internal VR Disabled  
High = Internal VR Enabled(Default)

U21A

FWH0/LAD0 K5 LPC\_AD0 LPC\_AD0 <37,40,45>  
FWH1/LAD1 K6 LPC\_AD1 LPC\_AD1 <37,40,45>  
FWH2/LAD2 K7 LPC\_AD2 LPC\_AD2 <37,40,45>  
FWH3/LAD3 K2 LPC\_AD3 LPC\_AD3 <37,40,45>

FWH4/LFRAME# K3 LPC\_FRAME# LPC\_FRAME# <37,40,45>

LDRQ0# J1 X  
LDRQ1# GPIO23 X

A20GATE A20M# N7 GATEA20 H\_A20M# GATEA20 <37>  
AJ27 H\_A20M# R848 2 8.2K\_0402\_5% +3VS

DPRSTP# AJ25 DPRSTP# R851 1 2 0.0402\_5% H\_DPRSTP# H\_DPRSTP# <6,8,54>  
DPSLP# AE23 DPSLP# R852 1 2 0.0402\_5% H\_DPSLP# H\_DPSLP# <6>

FERR# AJ26 FERR# R854 1 56\_0402\_5% H\_FERR# H\_FERR# <5>

CPUPWRGD AD22 H\_PWRGOOD H\_PWRGOOD <6>

IGNNE# AE25 H\_IGNNE# H\_IGNNE# <5>

INIT# AE22 H\_INIT# H\_INIT# <5>  
INTR RCIN# AG25 H\_INTR H\_INTR <5>  
KB\_RST# L3 KB\_RST# <37>

NMI SMIF# AF23 H\_NMI# H\_NMI# <5>  
AF24 H\_SMI# H\_SMI# <5>

STPCLK# AH27 H\_STPCLK# H\_STPCLK# <5>

THRMTrip# AG26 THRMTrip# R861 1 54.9\_0402\_1% H\_THERMTrip# H\_THERMTrip# <5,8>

TP12 AG27 X

SATA ODD

AH11 SATA\_DTX\_C\_IRX\_N4 T71 PAD @  
AJ11 SATA\_DTX\_C\_IRX\_P4 T72 PAD @  
AG12 SATA\_ITX\_DRX\_N4 T73 PAD @  
AF12 SATA\_ITX\_DRX\_P4 T75 PAD @

AH9 X  
AJ9 X  
AE10 X  
AF10 X

AH18 CLK\_PCIE\_SATA# CLK\_PCIE\_SATA# <23>  
AJ18 CLK\_PCIE\_SATA# CLK\_PCIE\_SATA# <23>  
AJ7 SATARBIAS  
AH7 R866 2 24.9\_0402\_1%

4mils width less than 500mils

SATA4RXN AH11 SATA\_DTX\_C\_IRX\_N4  
SATA4RXP AJ11 SATA\_DTX\_C\_IRX\_P4  
SATA4TXN AG12 SATA\_ITX\_DRX\_N4  
SATA4TXP AF12 SATA\_ITX\_DRX\_P4

SATA5RXN AH9 X  
SATA5RXP AJ9 X  
SATA5TXN AE10 X  
SATA5TXP AF10 X

SATA\_CLKN AH18 CLK\_PCIE\_SATA#  
SATA\_CLKP AJ18 CLK\_PCIE\_SATA#  
SATARBIAS AJ7  
AH7

MAINPWON <48,50>

R864 @ 330\_0402\_5%  
Q65  
2SC2411K\_SOT23 @

H\_THERMTrip#

Need check

GPIO56

12/8 Add by Vivian  
12/8 Close to RAM socket.

12/7 Modified X4 to SJ100001U00 10ppm

Flash Descriptor Security Override Strap

GPIO33 Low= Descriptor Security override  
High= Default\* (Internal pull-up)

XOR Chain Entrance Strap

| ICH_TP3 | HDA_SDOUT | Description                |
|---------|-----------|----------------------------|
| 0       | 0         | RSVD                       |
| 0       | 1         | Enter XOR Chain            |
| 1       | 0         | Normal Operation           |
| 1       | 1         | Set PCIE port config bit 1 |

Security Classification

Compal Secret Data

Issued Date 2008/07/15

Deciphered Date 2009/7/15

Title

Compal Electronics, Inc.

ICH9M(2/4)-LAN, IDELPC, RTC

Size Document Number

Custom KHLBX MB Schematic

Date: Monday, January 19, 2009

Sheet 28 of 56

Rev 1.0

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12/7 Modified X4 to SJ100001U00 10ppm

IC9M Internal VR Enable Strap  
(Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)

ICH\_INTVRMEN Low = Internal VR Disabled  
High = Internal VR Enabled(Default)

ICH9M LAN100 SLP Strap  
(Internal VR for VccLAN1.05 and VccCL1.05)

ICH\_LAN100\_SLP Low = Internal VR Disabled  
High = Internal VR Enabled(Default)

U21A

FWH0/LAD0 K5 LPC\_AD0 LPC\_AD0 <37,40,45>  
FWH1/LAD1 K6 LPC\_AD1 LPC\_AD1 <37,40,45>  
FWH2/LAD2 K7 LPC\_AD2 LPC\_AD2 <37,40,45>  
FWH3/LAD3 K2 LPC\_AD3 LPC\_AD3 <37,40,45>

FWH4/LFRAME# K3 LPC\_FRAME# LPC\_FRAME# <37,40,45>

LDRQ0# J1 X  
LDRQ1# GPIO23 X

A20GATE A20M# N7 GATEA20 H\_A20M# GATEA20 <37>  
AJ27 H\_A20M# R848 2 8.2K\_0402\_5% +3VS

DPRSTP# AJ25 DPRSTP# R851 1 2 0.0402\_5% H\_DPRSTP# H\_DPRSTP# <6,8,54>  
DPSLP# AE23 DPSLP# R852 1 2 0.0402\_5% H\_DPSLP# H\_DPSLP# <6>

FERR# AJ26 FERR# R854 1 56\_0402\_5% H\_FERR# H\_FERR# <5>

CPUPWRGD AD22 H\_PWRGOOD H\_PWRGOOD <6>

IGNNE# AE25 H\_IGNNE# H\_IGNNE# <5>

INIT# AE22 H\_INIT# H\_INIT# <5>  
INTR RCIN# AG25 H\_INTR H\_INTR <5>  
KB\_RST# L3 KB\_RST# <37>

NMI SMIF# AF23 H\_NMI# H\_NMI# <5>  
AF24 H\_SMI# H\_SMI# <5>

STPCLK# AH27 H\_STPCLK# H\_STPCLK# <5>

THRMTrip# AG26 THRMTrip# ICH# R861 1 2 54.9\_0402\_1% H\_THERMTrip# H\_THERMTrip# <5,8>

TP12 AG27 X

SATA ODD

AH11 SATA\_DTX\_C\_IRX\_N4 T71 PAD @  
AJ11 SATA\_DTX\_C\_IRX\_P4 T72 PAD @  
AG12 SATA\_ITX\_DRX\_N4 T73 PAD @  
AF12 SATA\_ITX\_DRX\_P4 T75 PAD @

SATA6RXN AH9 X  
SATA5RXP AJ9 X  
SATA5TXN AE10 X  
SATA5TXP AE10 X

SATA\_CLKN AH18 CLK\_PCIE\_SATA# CLK\_PCIE\_SATA# <23>  
SATA\_CLKP AJ18 CLK\_PCIE\_SATA CLK\_PCIE\_SATA <23>  
SATA6BIAS AH7 X  
SATA6BIAS R866 2 24.9\_0402\_1%

4mils width less than 500mils

MAINPWON <48,50>

R864 330\_0402\_5% Q65 2SC2411K\_SOT23 @  
H\_THERMTrip#

Need check

GPIO33

Low= Descriptor Security override  
High= Default\* (Internal pull-up)

XOR Chain Entrance Strap

| ICH_TP3 | HDA_SDOOUT | Description                |
|---------|------------|----------------------------|
| 0       | 0          | RSVD                       |
| 0       | 1          | Enter XOR Chain            |
| 1       | 0          | Normal Operation           |
| 1       | 1          | Set PCIE port config bit 1 |

Flash Descriptor Security Override Strap

GPIO33

Low= Descriptor Security override  
High= Default\* (Internal pull-up)

XOR Chain Entrance Strap

| ICH_TP3 | HDA_SDOOUT | Description                |
|---------|------------|----------------------------|
| 0       | 0          | RSVD                       |
| 0       | 1          | Enter XOR Chain            |
| 1       | 0          | Normal Operation           |
| 1       | 1          | Set PCIE port config bit 1 |

Security Classification

Compal Secret Data

Issued Date

2008/07/15

Deciphered Date

2009/7/15

Title

Compal Electronics, Inc.

ICH9M(2/4)-LAN, IDELPC, RTC

Size

Document Number

KHLBX MB Schematic

Rev

1.0

Date

Monday, January 19, 2009

Sheet

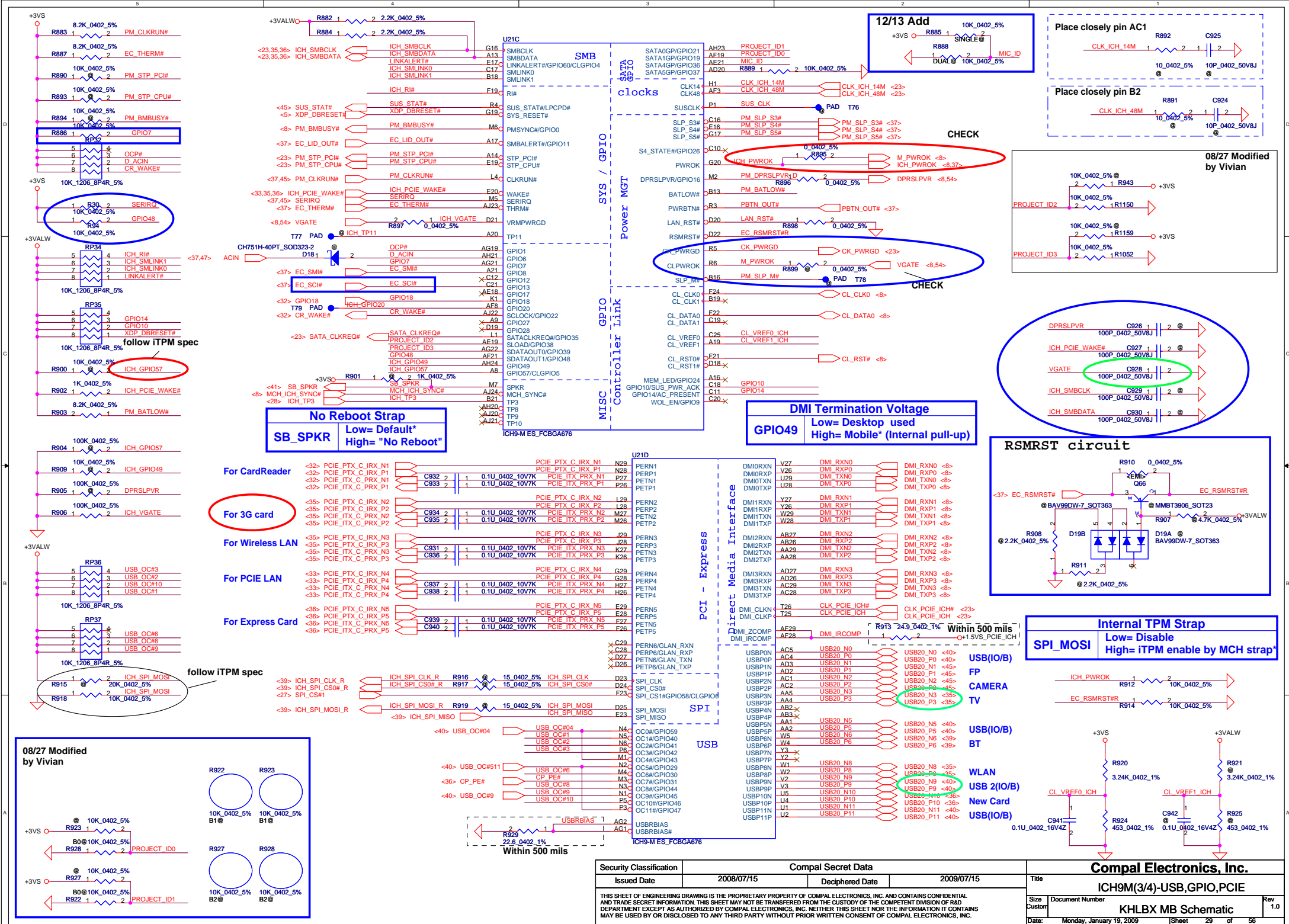
28

of

56

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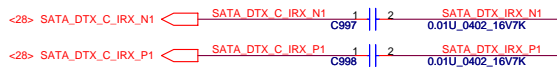
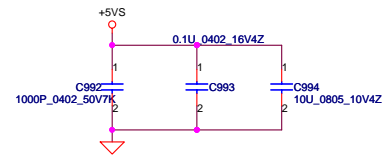


|   |                    |                 |            |  |  |  |  |
|---|--------------------|-----------------|------------|--|--|--|--|
| Security Classification   | Compal Secret Data |                 |            | <div> <div>Compal Electronics, Inc.</div> <div> <div> <div>Title</div> <div>ICH9M(3/4)-USB,GPIO,PCIE</div> </div> <div> <div>Size Custom</div> <div>Document Number</div> </div> <div> <div>KHLBX MB Schematic</div> <div> <div>Date: Monday, January 19, 2009</div> <div> <div>Sheet 29 of 56</div> <div>Rev 1.0</div> </div> </div> </div> </div> </div> |  |  |  |
| Issued Date   | 2008/07/15         | Deciphered Date | 2009/07/15 |  |  |  |  |
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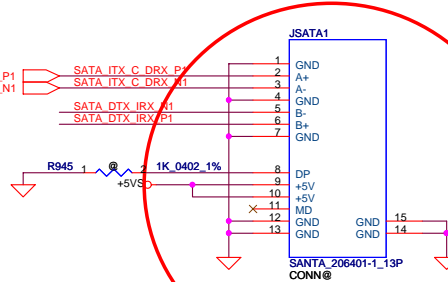




## SATA ODD Conn.

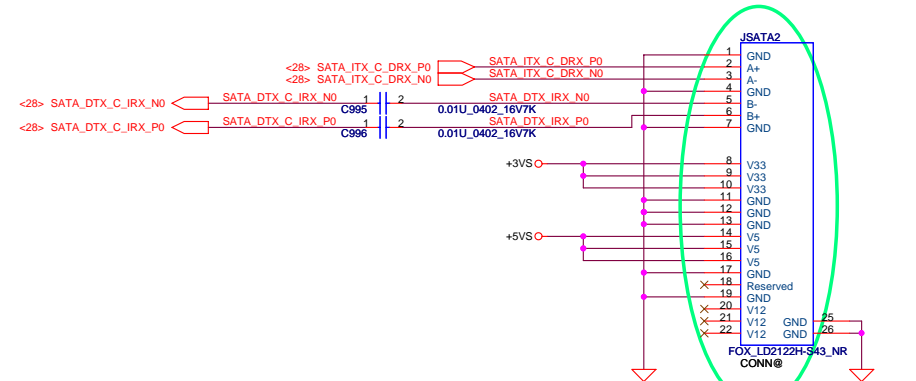
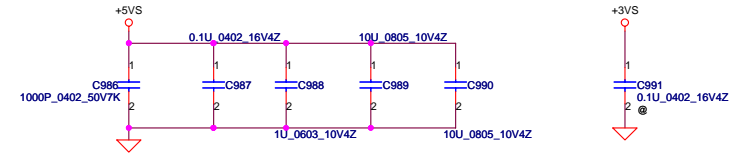


Copy JAL90 Symbol



Need check layout !!

## SATA HDD Conn.

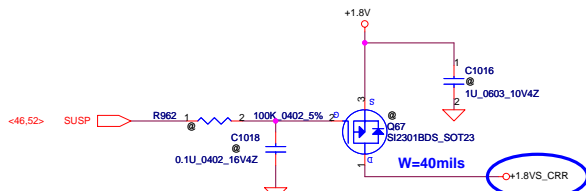
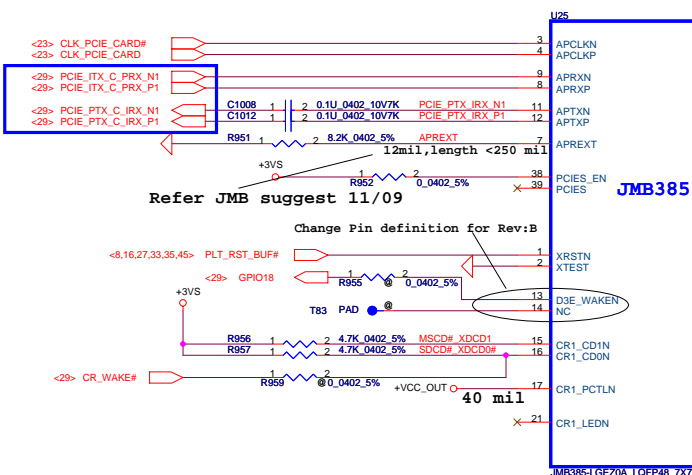
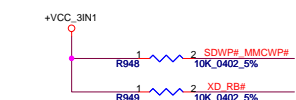


(NEW)

Change Library  
Update Symbol  
SP01000G800  
FOX\_LD2122H-S43\_NR  
Manually update pin number

|   |            |                    |            |                                |                 |
|---|------------|--------------------|------------|--------------------------------|-----------------|
| Security Classification   |            | Compal Secret Data |            | Compal Electronics, Inc.       |                 |
| Issued Date   | 2008/07/15 | Deciphered Date    | 2009/07/15 | Title                          |                 |
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|   |            |                    |            | KHLBX MB Schematic             |                 |
|   |            |                    |            | Date: Monday, January 19, 2009 | Sheet 31 of 56  |
|   |            |                    |            | Rev 1.0                        |                 |

Diagram illustrating a voltage divider circuit for VCC\_OUT. The circuit consists of a resistor R946 (0.0805, 5%) in series with a capacitor C1001 (10u, 0.0805, 10V4Z). This is followed by a parallel combination of a capacitor C1002 (0.1u, 0.0402, 16V4Z) and the output node VCC\_OUT. The input is VCC\_3IN1. A red circle highlights the resistor R946 and the capacitor C1001. A note "mount JMB suggest" points to the capacitor C1001.



11/24 Andy

40mil

3V3

+VCC\_OUT

U24

VIN VOUT

VIN/VCC VOUT

1 5

3 4

2

GND

RT9701-PB\_SOT23-5

+VCC\_3IN1

C999

0.1uF\_0402\_16V4Z

C1000

1uF\_0805\_10V4Z

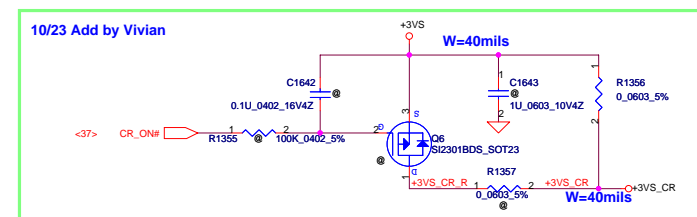
R947

150K\_0402\_5%

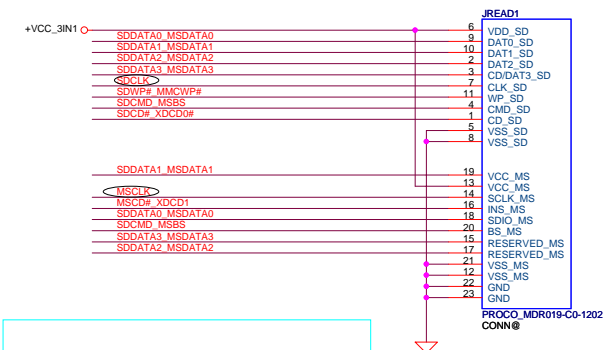
reserved power circuit

Refer JMB suggest 11/14

10/23 Change net name to +3VS\_CR by Vivian

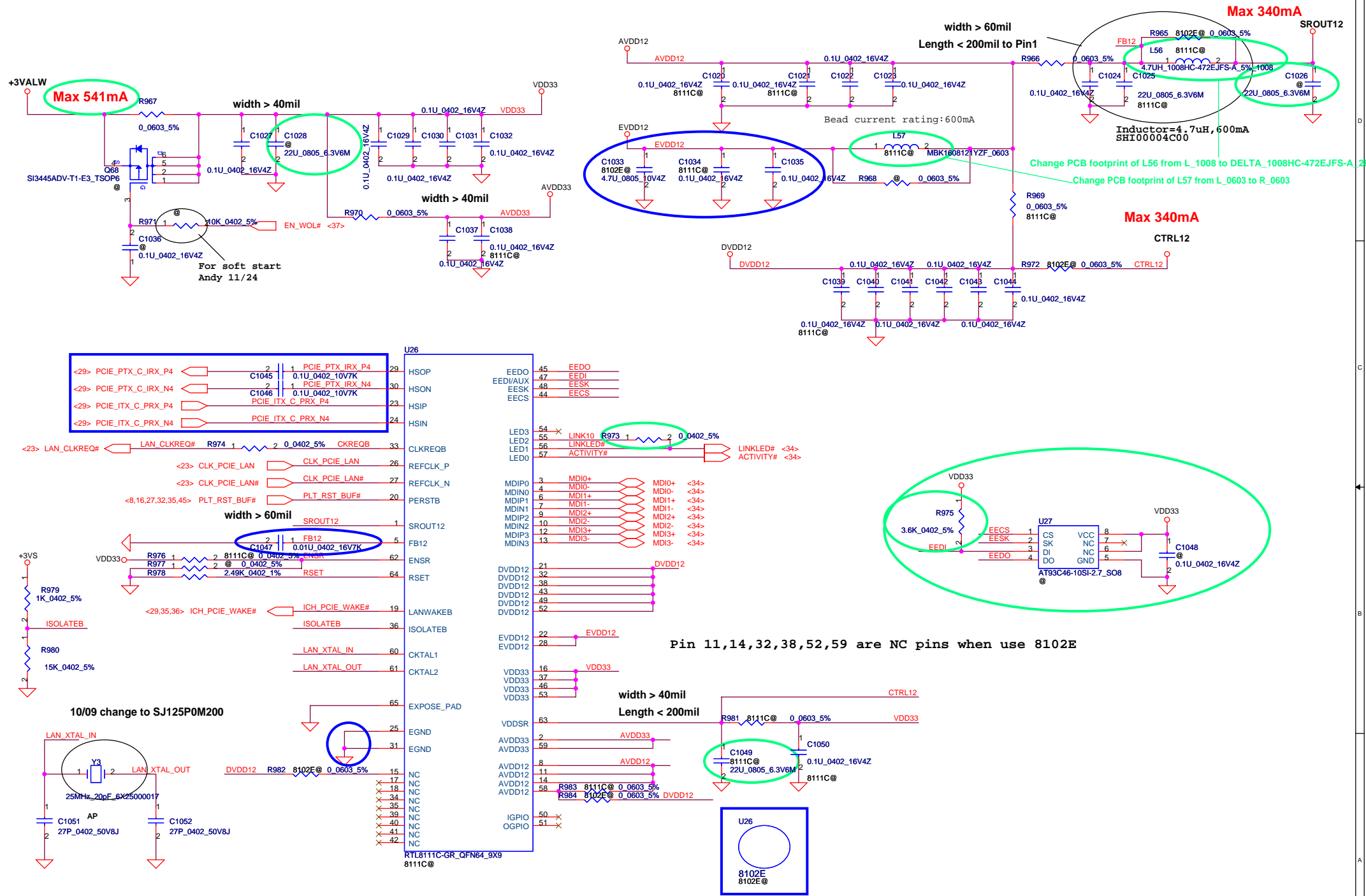


### 3 in 1 Card Reader

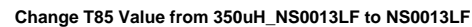
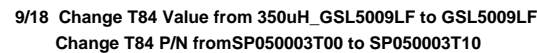


| SD,MMC,MS multi-function pin define |                         |                     |
|-------------------------------------|-------------------------|---------------------|
| MDIO<br>PIN Name                    | SD/MMC Card<br>PIN Name | MS Card<br>PIN Name |
| MDIO00                              | SD1_DAT0                | MS1_DAT0            |
| MDIO01                              | SD1_DAT1                | MS1_DAT1            |
| MDIO02                              | SD1_DAT2                | MS1_DAT2            |
| MDIO03                              | SD1_DAT3                | MS1_DAT3            |
| MDIO04                              | SD1_CMD                 | MS1_BS              |
| MDIO05                              | SD1_CLK                 | MS1_CLK             |
| MDIO06                              | SD1_WP                  |                     |
| MDIO07                              |                         |                     |
| MDIO08                              | MMC_DAT4                | MS1_DAT4            |
| MDIO09                              | MMC_DAT5                | MS1_DAT5            |
| MDIO10                              | MMC_DAT6                | MS1_DAT6            |
| MDIO11                              | MMC_DAT7                | MS1_DAT7            |
| MDIO12                              |                         |                     |
| MDIO13                              |                         |                     |
| MDIO14                              |                         |                     |
| CR1_LEDN                            | SD1_LED#                | MS1_LED#            |
| CR1_PCTLN                           | SD1_PCTL#               | MS1_PCTL#           |
| CR1_CD0                             | SD1_CD#                 |                     |
| CR1_CD1                             |                         | MS1_CD#             |

|   |            |                    |            |                          |                          |                |
|---|------------|--------------------|------------|--------------------------|--------------------------|----------------|
| Security Classification   |            | Compal Secret Data |            | Compal Electronics, Inc. |                          |                |
| Issued Date   | 2008/07/15 | Deciphered Date    | 2009/07/15 | Title                    | JMB385 CardReader        |                |
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|   |            |                    |            | Custom                   | KHLBX MB Schematic       | 1.             |
|   |            |                    |            | Date:                    | Monday, January 19, 2009 | Sheet 32 of 56 |



|   |                          |                    |            |                          |  |
|---|--------------------------|--------------------|------------|--------------------------|--|
| Security Classification   |                          | Compal Secret Data |            | Compal Electronics, Inc. |  |
| Issued Date   | 2008/07/15               | Deciphered Date    | 2009/07/15 | Title                    |  |
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| Size  | Document Number          | KHLBX MB Schematic |            | Rev                      |  |
| Custom  |                          |                    |            | 1.0                      |  |
| Date:   | Monday, January 19, 2009 | Sheet              | 33         | of 56                    |  |

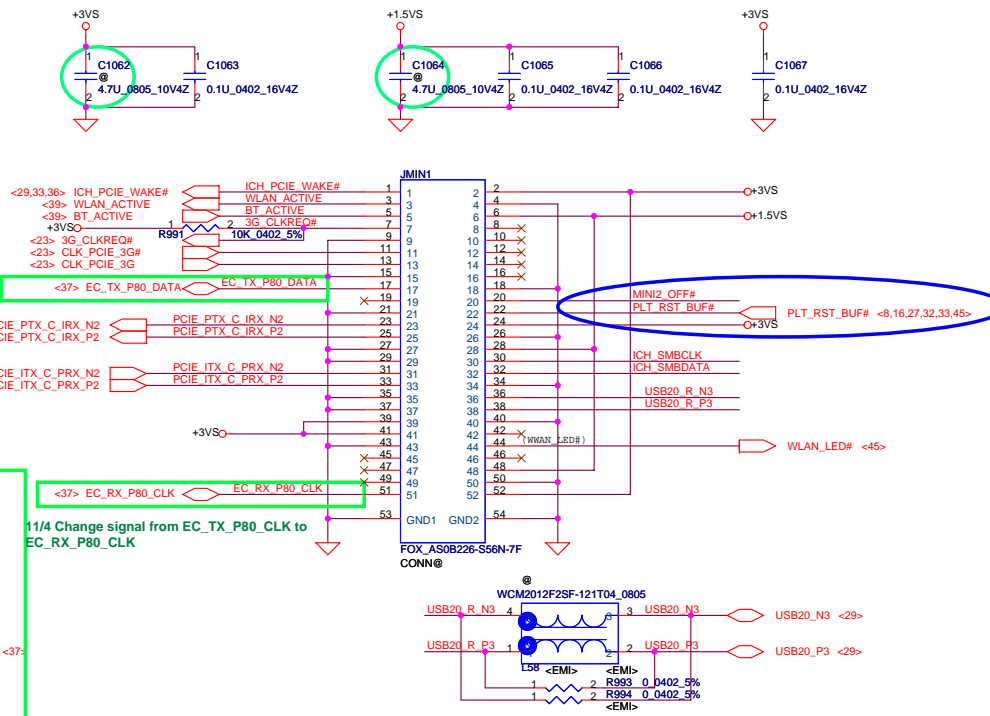
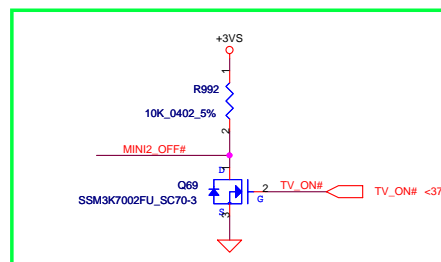


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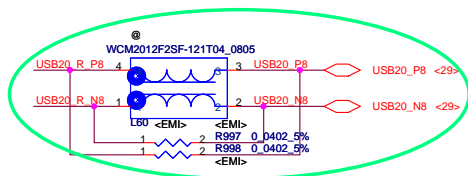
# Mini-Express Card for TV Tuner

Vcc 3.3V +/- 8%  
Peak Icc 2750mA  
with max supply droop 50mA  
Average Icc 1000mA

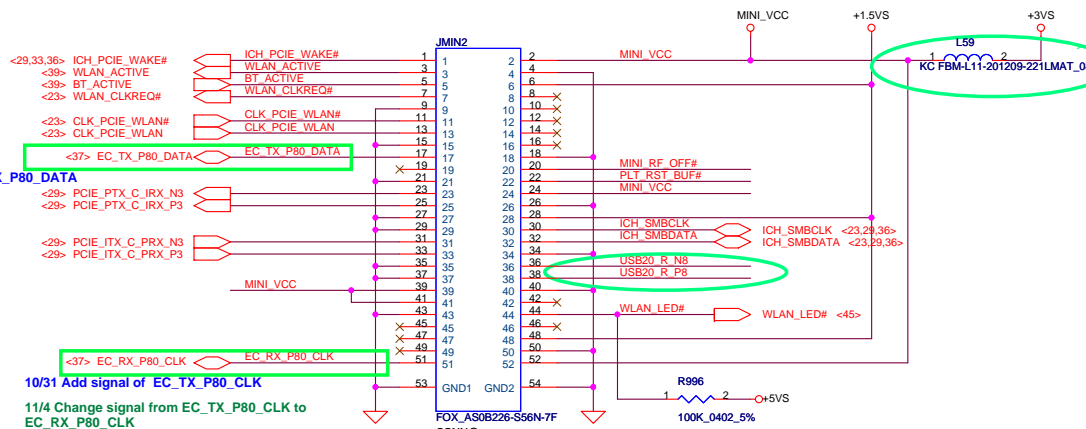
11/3 Change signal of EC\_TX\_P80\_DATA from pin 49 to pin 17



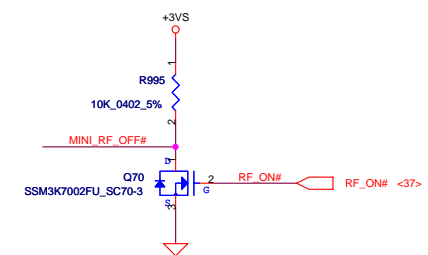
# Mini-Express Card for WLAN



10/31 Add signal of EC\_TX\_P80\_DATA



Change PCB footprint of L59 from L\_0805 to R\_0805



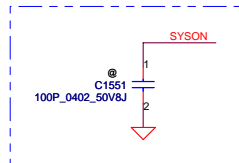
Please place these caps between JMIN1 and JMIN2

|             |       |   |   |                   |
|-------------|-------|---|---|-------------------|
| ICH_SMBCLK  | C1068 | 1 | 2 | @ 100P_0402_50V8J |
| ICH_SMBDATA | C1070 | 1 | 2 | @ 100P_0402_50V8J |

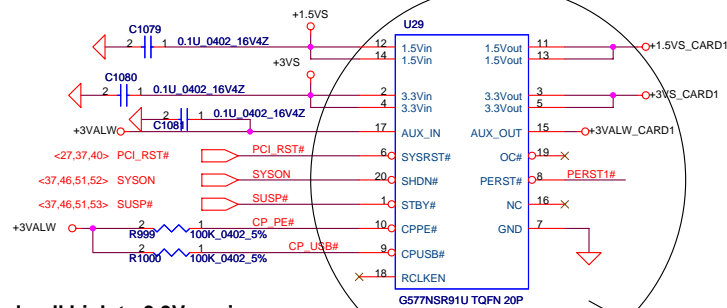
|  |  |                    |  |                 |  |                          |  |                       |  |                          |  |                |  |
|--|--|--------------------|--|-----------------|--|--------------------------|--|-----------------------|--|--------------------------|--|----------------|--|
| Security Classification  |  | Compal Secret Data |  |                 |  | Compal Electronics, Inc. |  |                       |  |                          |  |                |  |
| Issued Date  |  | 2008/07/15         |  | Deciphered Date |  | 2009/07/15               |  | Title                 |  |                          |  |                |  |
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|  |  |                    |  |                 |  |                          |  | Size                  |  | Document Number          |  | Rev            |  |
|  |  |                    |  |                 |  |                          |  |                       |  | KHLBX MB Schematic       |  | 1.0            |  |
|  |  |                    |  |                 |  |                          |  | Date:                 |  | Monday, January 19, 2009 |  | Sheet 35 of 56 |  |

## New Card Power Switch

## New Card



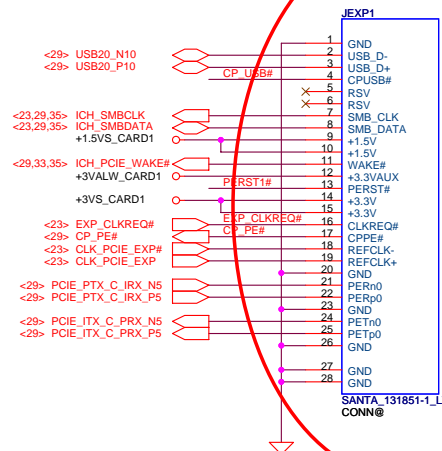
internal pull high to 3.3Vaux-in  
EC need setting at Hi-Z & output Low



10/20 Change to value to G577NSR91U TQFN 20P

## New Card Socket (Left/TOP)

Copied from HAL10

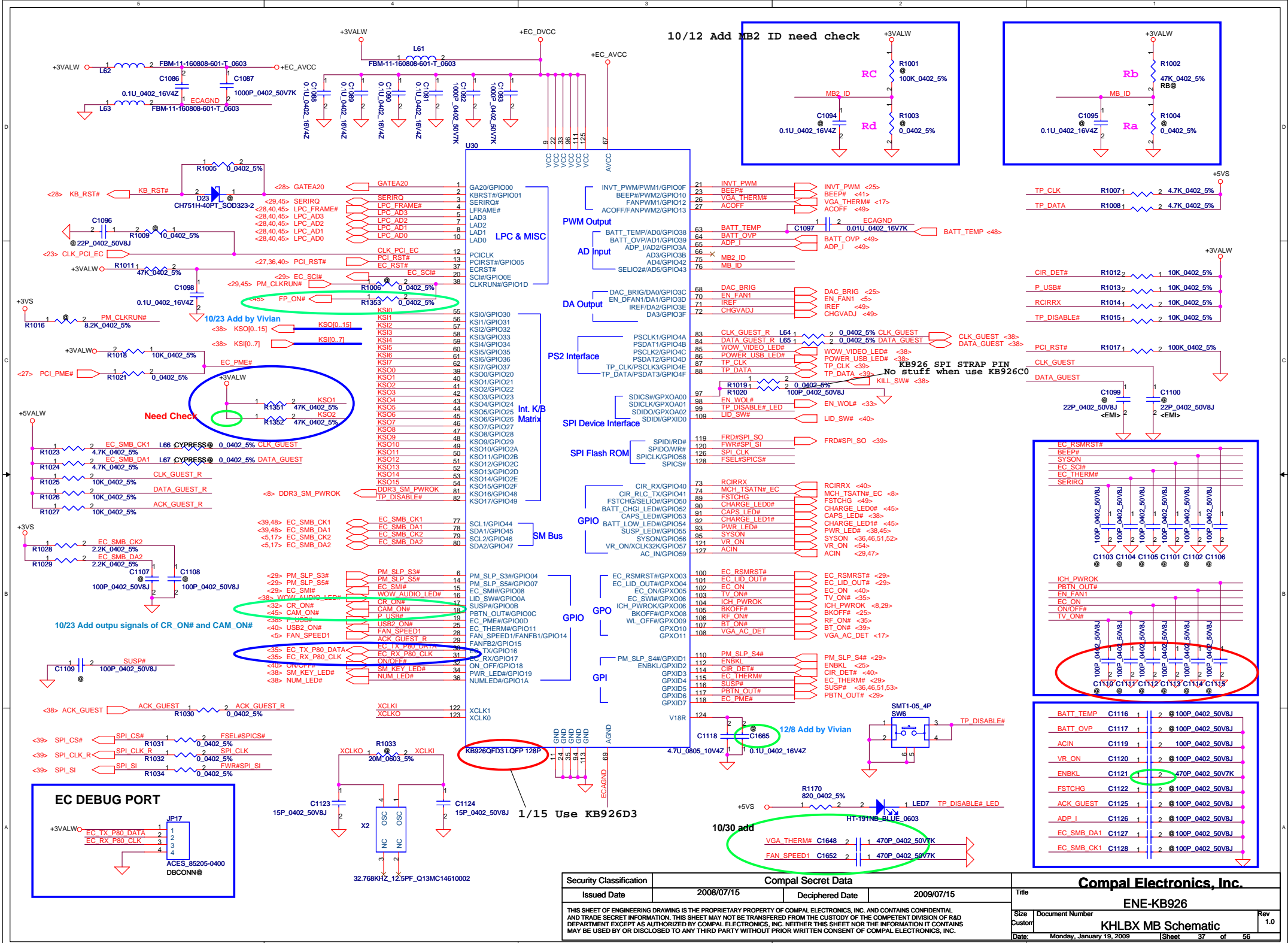


Need checking layout !!

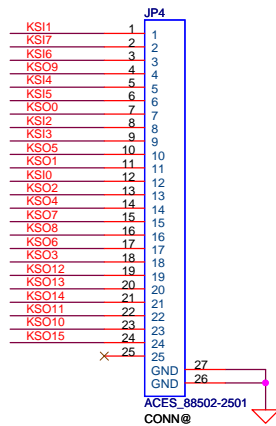
Change connector from SANTA\_130810-1 to SANTA\_13185-1\_LT

|   |            |                    |            |                                |                 |
|---|------------|--------------------|------------|--------------------------------|-----------------|
| Security Classification   |            | Compal Secret Data |            | Compal Electronics, Inc.       |                 |
| Issued Date   | 2008/07/15 | Deciphered Date    | 2009/07/15 | Title                          | NEW CARD        |
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|   |            |                    |            | KHLBX MB Schematic             |                 |
|   |            |                    |            | Date: Monday, January 13, 2009 | Rev 1.0         |
|   |            |                    |            | Sheet 36 of 56                 |                 |

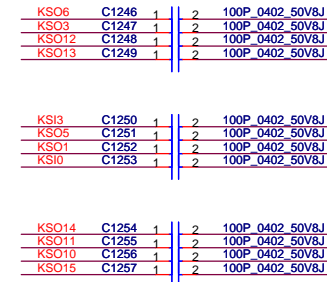
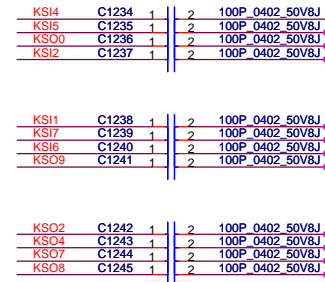




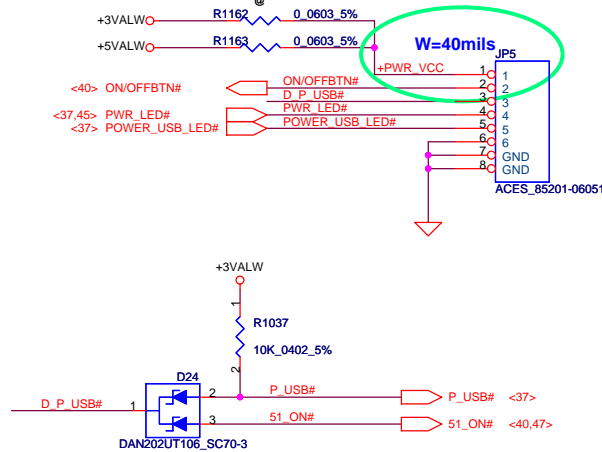
## INT\_KBD Conn.



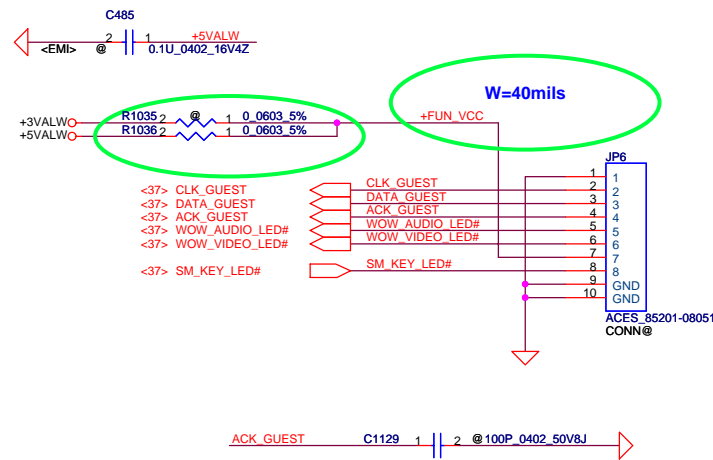
KSII[0..7] <37>  
KSO[0..15] <37>



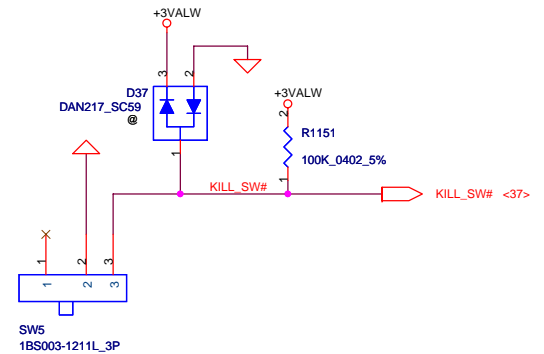
## Power USB Board Conn



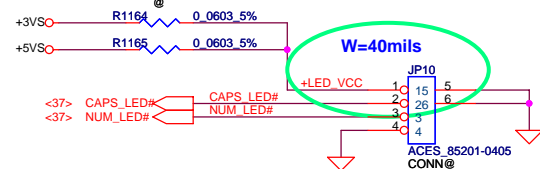
## Fun conn



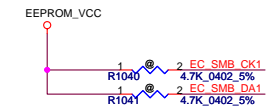
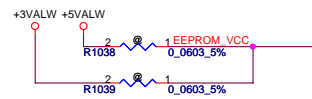
## Kill SWITCH



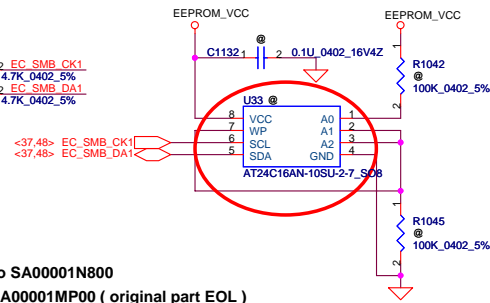
## LED Board Conn



|   |                          |                    |            |                          |  |
|---|--------------------------|--------------------|------------|--------------------------|--|
| Security Classification   |                          | Compal Secret Data |            | Compal Electronics, Inc. |  |
| Issued Date   | 2008/07/15               | Deciphered Date    | 2009/07/15 | Title                    |  |
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| Size B  | Document Number          | KHLBX MB Schematic |            | Rev 1.0                  |  |
| Date:   | Monday, January 19, 2009 | Sheet              | 38 of 56   |                          |  |



12/28 Add

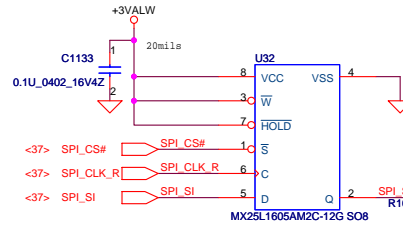


0206 ==> change PN to SA00001N800

12/19 change pn to SA00001MP00 ( original part EOL )

12/25 change back to SA024160140 ( Samples can not on time )

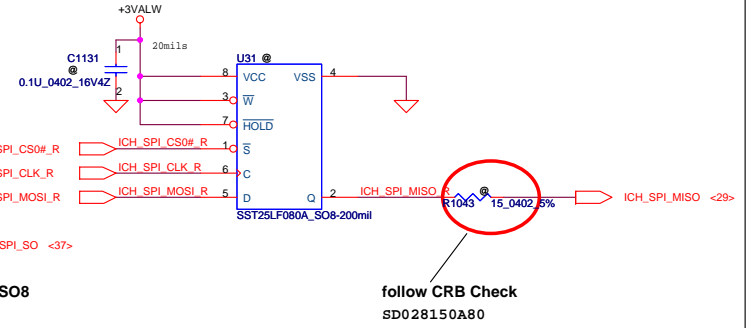
## 16M SPI ROM For EC+BIOS+VBIOS



10/20 Change value of U32 to MX25L1605AM2C-12G SO8

12/15 change from 15 to 0 ohm'

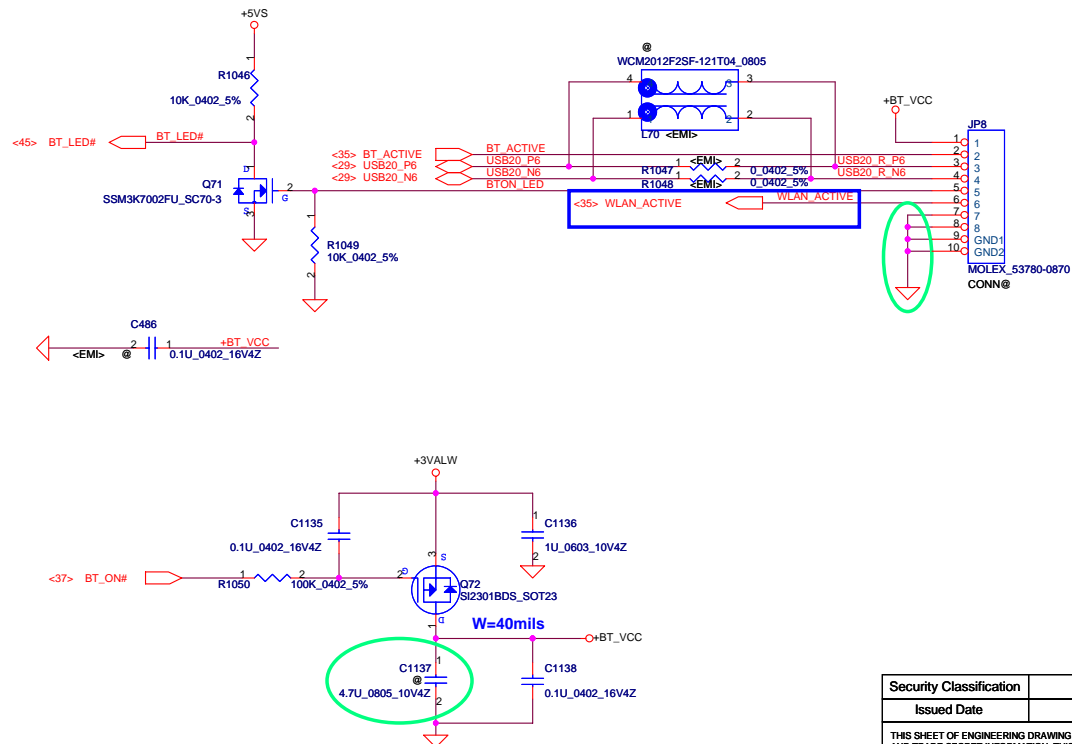
## 8M SPI ROM For iTPM+HDCP



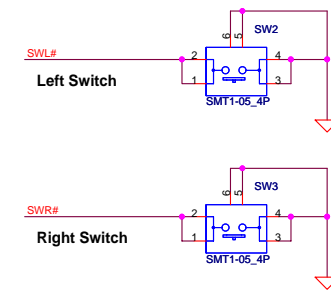
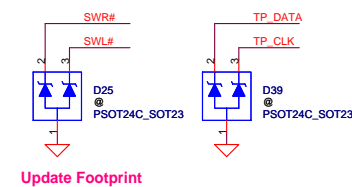
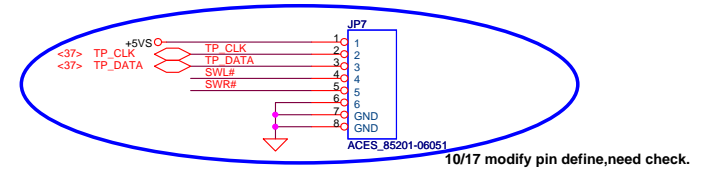
## Bluetooth Conn.

Need to check BT pin definition again!

9/20 modified this block

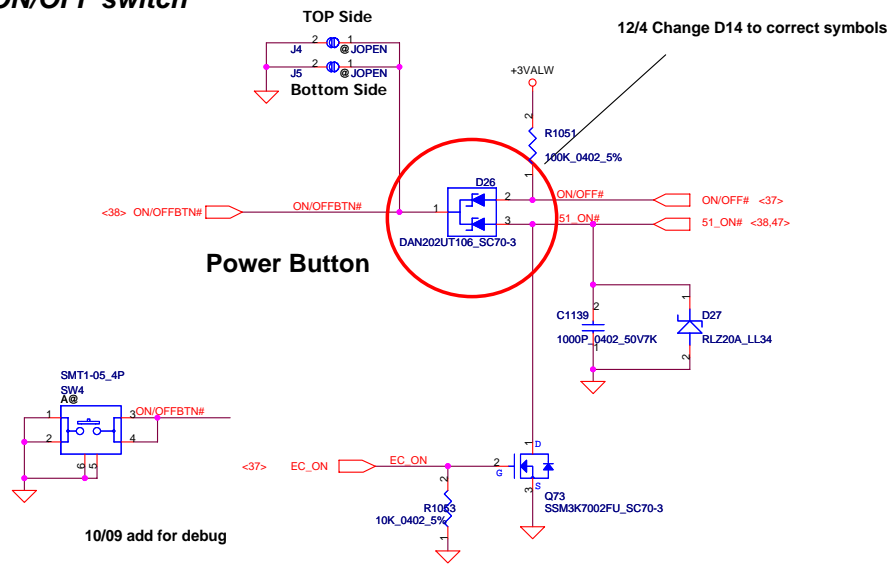


## To TP/B Conn.

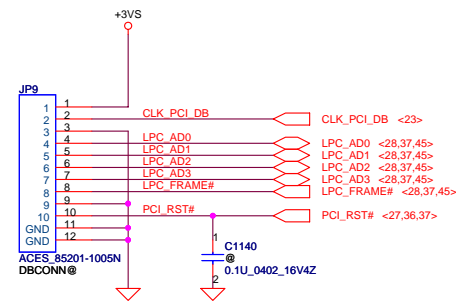


|   |  |                    |  |                 |  |                          |  |       |                    |                          |     |                |
|---|--|--------------------|--|-----------------|--|--------------------------|--|-------|--------------------|--------------------------|-----|----------------|
| Security Classification   |  | Compal Secret Data |  |                 |  | Compal Electronics, Inc. |  |       |                    |                          |     |                |
| Issued Date   |  | 2008/07/15         |  | Deciphered Date |  | 2009/07/15               |  | Title |                    | BIOS, TP & BT Connector  |     |                |
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|   |  |                    |  |                 |  |                          |  |       | KHLBX MB Schematic |                          | 1.0 |                |
|   |  |                    |  |                 |  |                          |  |       |                    |                          |     |                |
|   |  |                    |  |                 |  |                          |  | Date: |                    | Monday, January 19, 2009 |     | Sheet 39 of 56 |

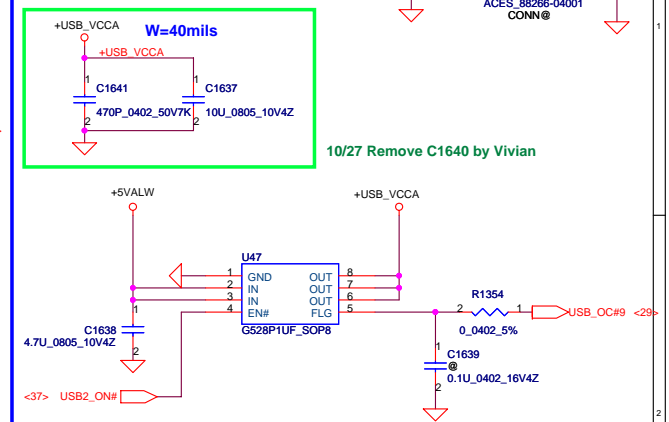
## ON/OFF switch



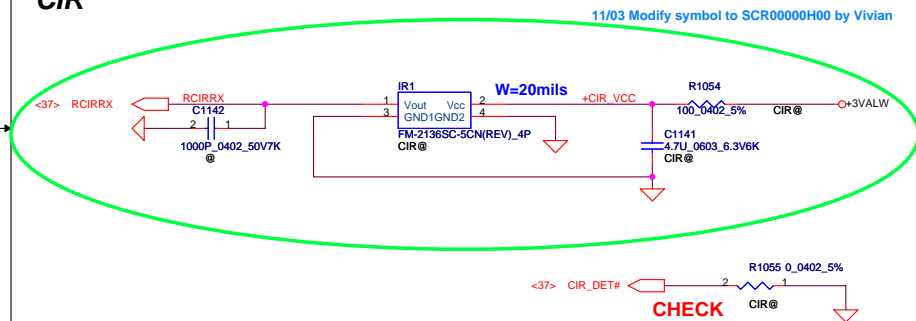
## FOR LPC DEBUG PORT



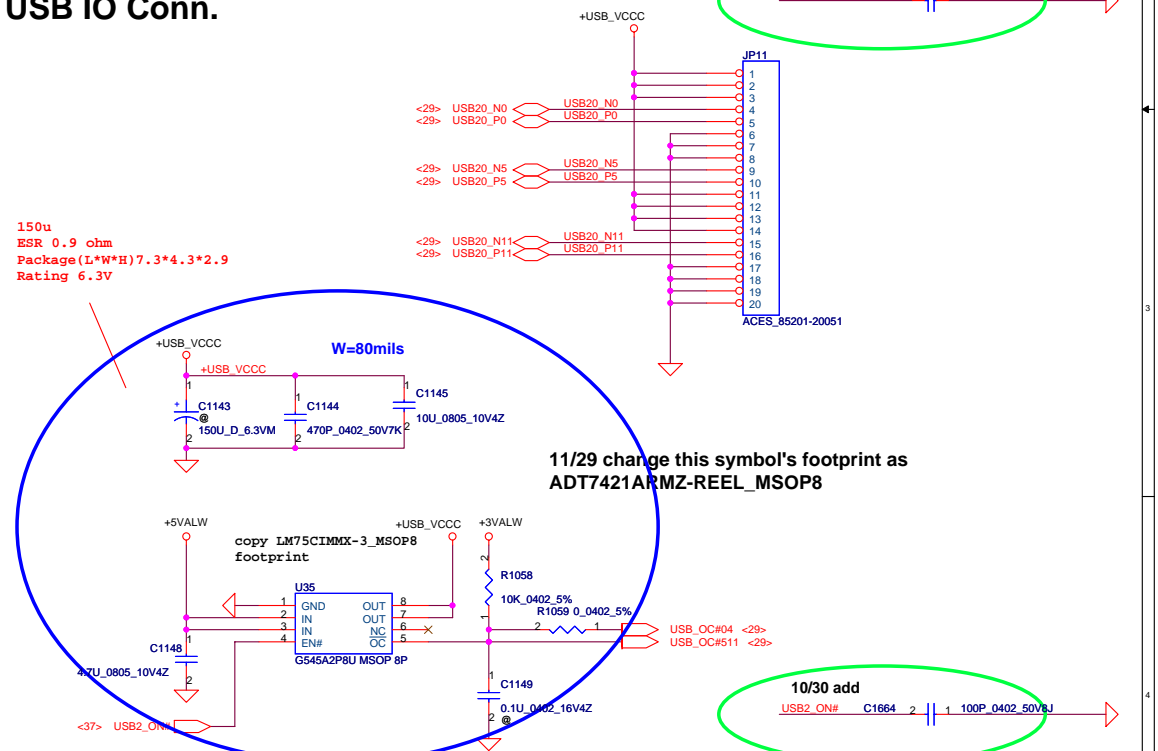
## USB IO 2 Conn.



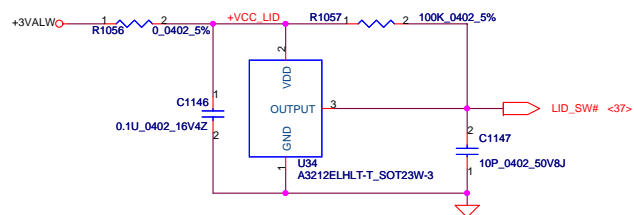
## CIR



## USB IO Conn.



## Lid Switch



| Security Classification   |                          | Compal Secret Data |            | Compal Electronics, Inc.      |     |
|---|--------------------------|--------------------|------------|-------------------------------|-----|
| Issued Date   | 2008/07/15               | Deciphered Date    | 2009/07/15 | Title                         |     |
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| Size B  | Document Number          | KHLBX MB Schematic |            | Rev                           | 1.0 |
| Date:   | Monday, January 19, 2009 | Sheet              | 40         | of                            | 56  |

**HD Audio Codec**

**EC Beep**

**PCI Beep**

**Regulator for CODEC**

**Moat Bridge**

**ESD**

**SENSE FOR Ext. Mic.**

**SENSE FOR Solo Int. Mic.**

**SENSE FOR HP**

**Table:**

| Sense Pin   | Impedance | Codec Signals       | Function |
|-------------|-----------|---------------------|----------|
| SENSE A / B | 39.2K     | PORT-A (PIN 39, 41) | HP       |
|             | 20K       | PORT-B (PIN 21, 22) | MIC      |
|             | 10K       | PORT-C (PIN 23, 24) | LINE IN  |
| SENSE B     | 5.1K      | PORT-D (PIN 35, 36) | LINE OUT |
|             | 39.2K     | PORT-E (PIN 14, 15) | HP       |
|             | 20K       | PORT-F (PIN 16, 17) | MIC      |
|             | 10K       | PORT-G (PIN 43, 44) | LINE IN  |
|             | 5.1K      | PORT-H (PIN 45, 46) | LINE OUT |

**Table:**

| Security Classification | Compal Secret Data |                 | Date       |  |
|-------------------------|--------------------|-----------------|------------|--|
| Issued Date             | 2008/07/15         | Deciphered Date | 2009/07/15 |  |

**Table:**

| Compal Electronics, Inc. |                          |                |
|--------------------------|--------------------------|----------------|
| HD Audio Codec ALC268    |                          |                |
| Size Custom              | Document Number          | Rev            |
|                          | KHLBX MB Schematic       | 1.0            |
| Date:                    | Monday, January 19, 2009 | Sheet 41 of 56 |

**PCI Beep**

| Sense Pin   | Impedance | Codec Signals       | Funnnction |
|-------------|-----------|---------------------|------------|
| SENSE A / B | 39.2K     | PORT-A (PIN 39, 41) | HP         |
|             | 20K       | PORT-B (PIN 21, 22) | MIC        |
|             | 10K       | PORT-C (PIN 23, 24) | LINE IN    |
|             | 5.1K      | PORT-D (PIN 35, 36) | LINE OUT   |
| SENSE B     | 39.2K     | PORT-E (PIN 14, 15) | HP         |
|             | 20K       | PORT-F (PIN 16, 17) | MIC        |
|             | 10K       | PORT-G (PIN 43, 44) | LINE IN    |
|             | 5.1K      | PORT-H (PIN 45, 46) | LINE OUT   |

### Regulator for CODEC

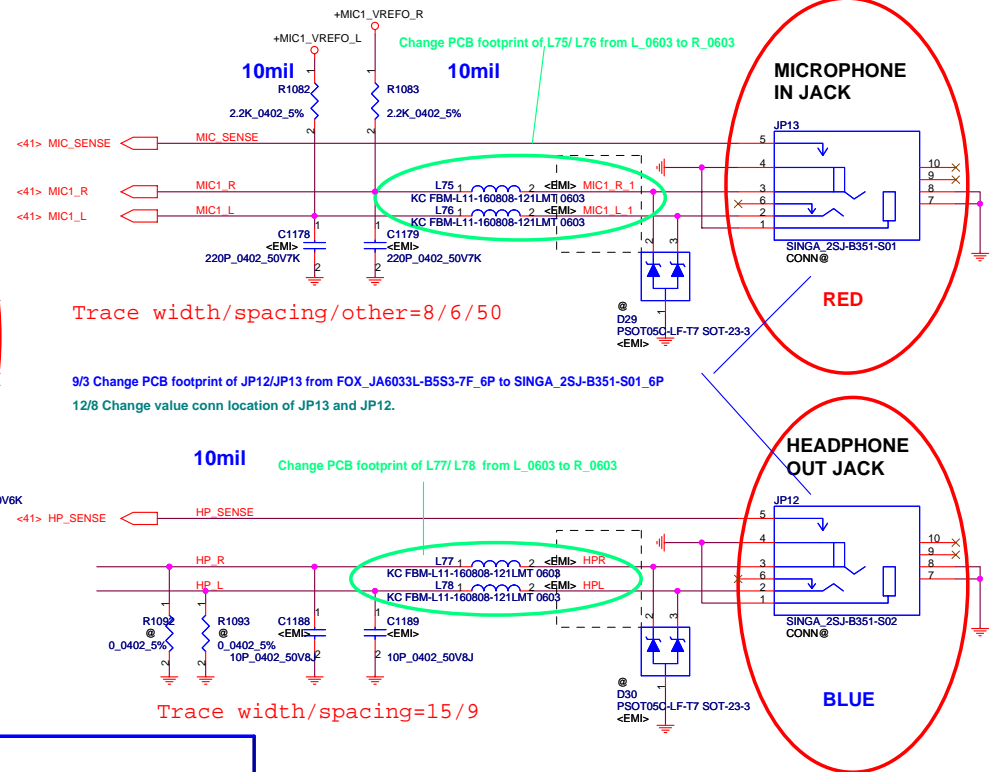
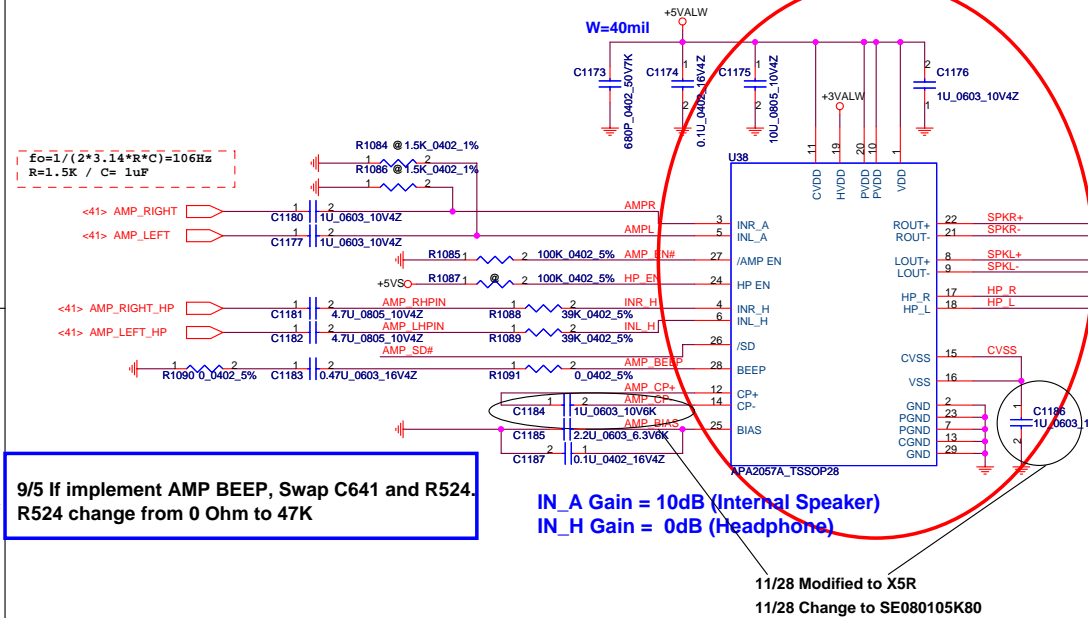
10/2 change circuit  
10/17 Change GND to digital

U8 change footprint

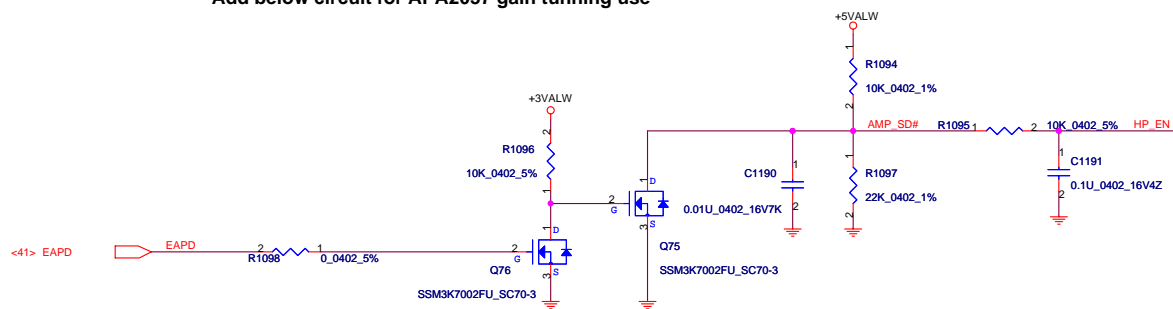
|   |            |                    |            |                                |                    |  |            |                          |                |
|---|------------|--------------------|------------|--------------------------------|--------------------|--|------------|--------------------------|----------------|
| Security Classification   |            | Compal Secret Data |            | Compal Electronics, Inc.       |                    |  |            |                          |                |
| Issued Date   | 2008/07/15 | Deciphered Date    | 2009/07/15 | Title<br>HD Audio Codec ALC268 |                    |  |            |                          |                |
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|   |            |                    |            | Custom                         | KHLBX MB Schematic |  |            |                          |                |
|   |            |                    |            | Date:                          |                    |  |            | Monday, January 19, 2009 | Sheet 41 of 56 |

# APA2057 SPK/HP Amplifier

10/2 U6 APA2057A P/N:SA00001QD00

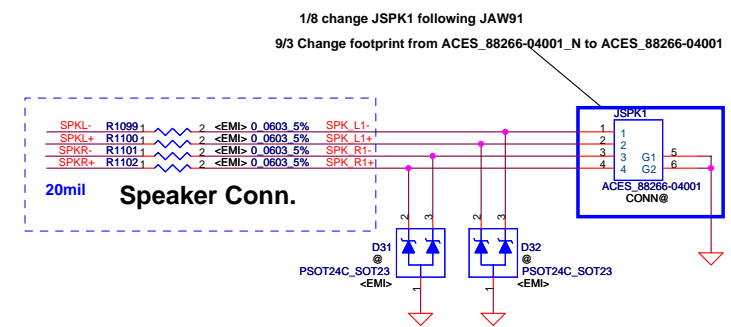
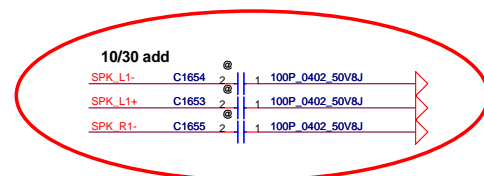


Add below circuit for APA2057 gain tuning use



| Gain (dB) | Low (V) | High (V) | Recommended (V) |
|-----------|---------|----------|-----------------|
| 10        | 3.45    | 3.51     | 3.48            |
| 11        | 3.56    | 3.62     | 3.59            |
| 12        | 3.68    | 3.73     | 3.70            |
| 13        | 3.80    | 3.85     | 3.82            |

+5VALW assume equal 5.1V  
 10 dB ----> 5.1 x 220 / 320 = 3.5

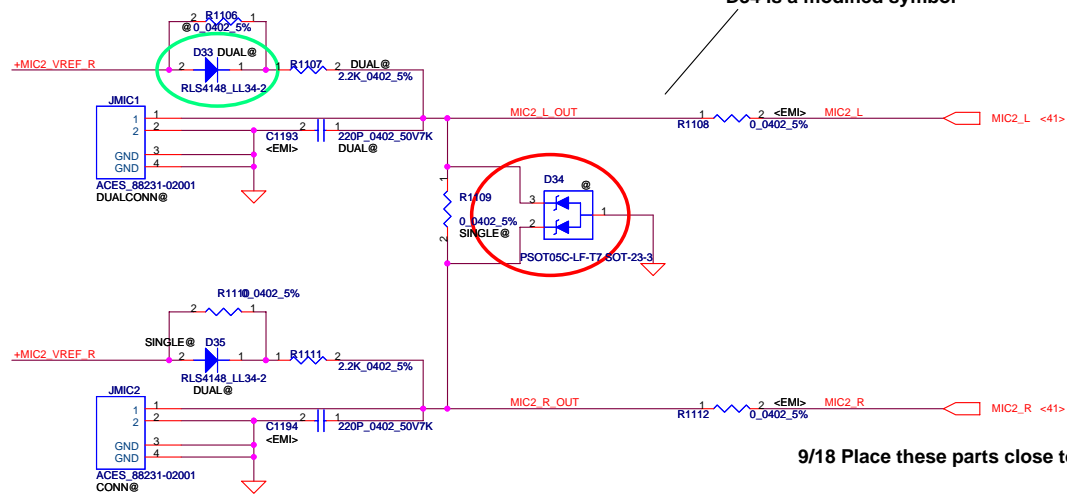


| Security Classification   |            |                 | Compal Secret Data |  |  | Title    |                          |                |
|---|------------|-----------------|--------------------|--|--|----------|--------------------------|----------------|
| Issued Date   | 2008/07/15 | Deciphered Date | 2009/07/15         |  |  | Size     | Document Number          | Rev            |
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|   |            |                 |                    |  |  | Date:    | Monday, January 19, 2009 | Sheet 42 of 56 |



The circuit diagram shows the connection of the MIC2\_VREFO pin to the +MIC2\_VREF pin. A red trace labeled +MIC2\_VREFO connects to the MIC2\_VREFO pin. This trace continues as +MIC2\_VREF through resistor R1104 (0.0402\_5%) to a junction point. From this junction, one path goes through resistor R1103 (10K\_0402\_5%) to a +3VS supply, and another path goes through capacitor C1192 (0.1U\_0402\_16V4Z) and resistor R1105 (27K\_0402\_5%) to ground. The components are highlighted with green circles.

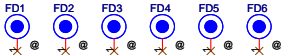
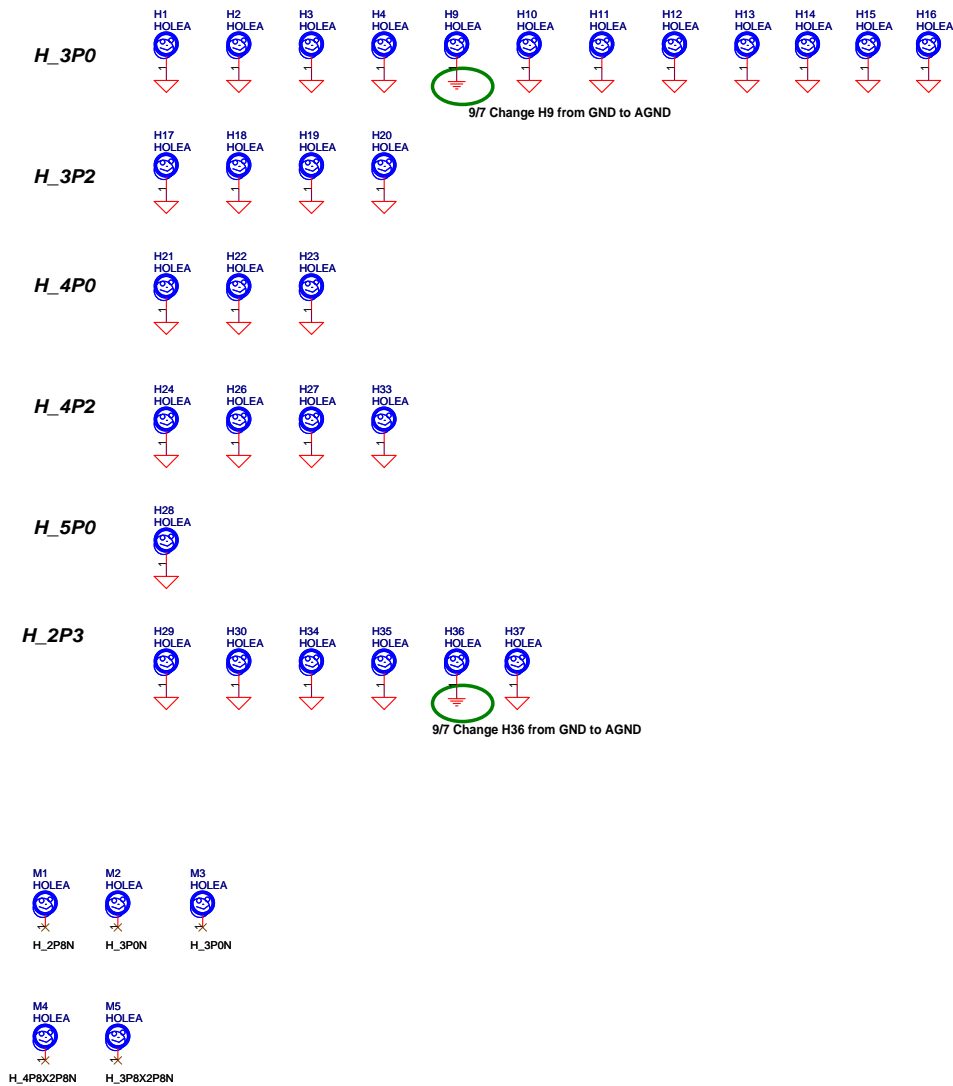
**D34 is a modified symbol**



**9/18 Place these parts close to CODEC (U36)**

|   |  |                    |                 |                          |  |                    |                          |  |       |     |     |
|---|--|--------------------|-----------------|--------------------------|--|--------------------|--------------------------|--|-------|-----|-----|
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|   |  |                    |                 |                          |  | Size               | Document Number          |  |       | Rev |     |
|   |  |                    |                 |                          |  | KHLBX MB Schematic |                          |  |       |     | 1.0 |
|   |  |                    |                 |                          |  | Date               | Monday, January 19, 2009 |  | Sheet | 43  | of  |

11/27 Add screw for layout request



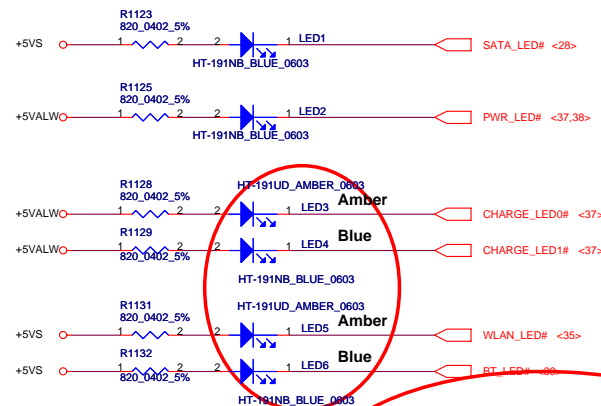
11/27 Add screw for layout request

|   |                    |                 |            |                                |                |
|---|--------------------|-----------------|------------|--------------------------------|----------------|
| Security Classification   | Compal Secret Data |                 |            | Compal Electronics, Inc.       |                |
| Issued Date   | 2008/07/15         | Deciphered Date | 2009/07/15 | Screw                          |                |
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|   |                    |                 |            | KHLBX MB Schematic             |                |
|   |                    |                 |            | Date: Monday, January 13, 2009 | Sheet 44 of 56 |

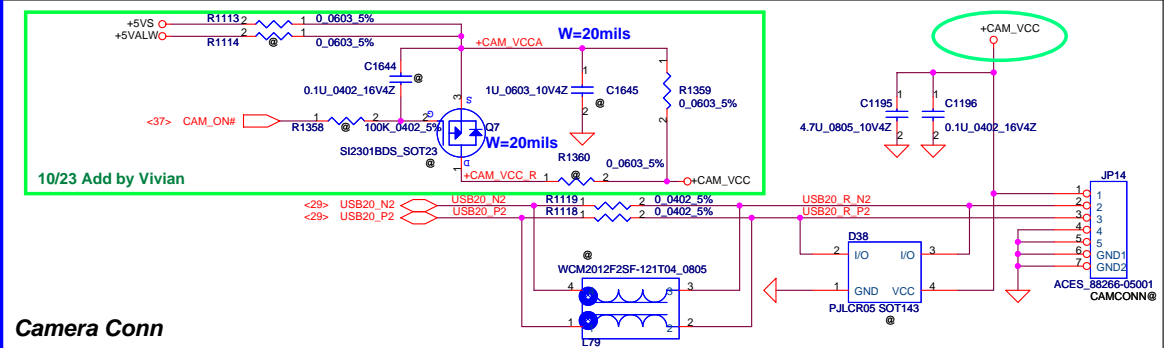
**LED**

## TPM X76 Information

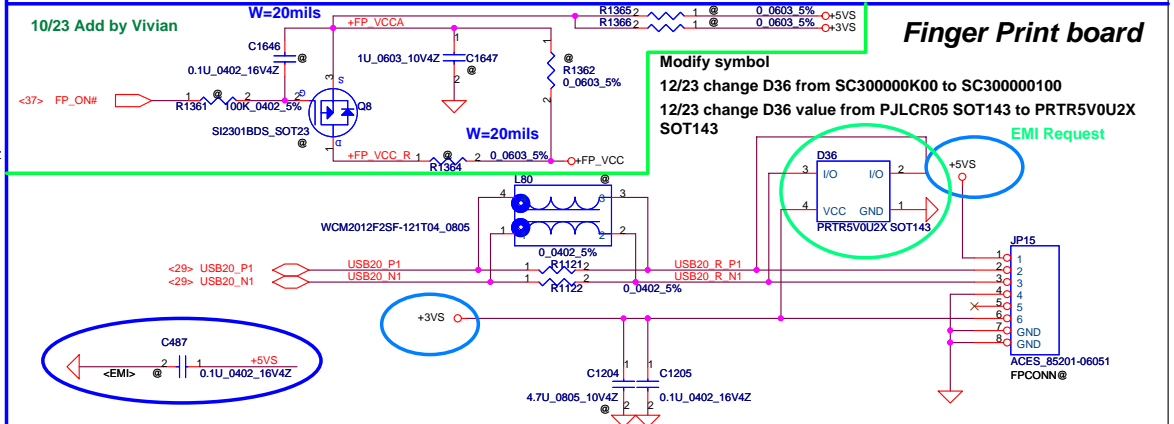
| X76 P/N     | Vendor   | Location                        | Bom Structure |
|-------------|----------|---------------------------------|---------------|
| X7611630L07 | Infineon | C717,C718,R698,R702,R703,U32,X3 | IN_TPM@       |
| X7611630L08 | Winbond  | C724,U32                        | WB_TPM@       |



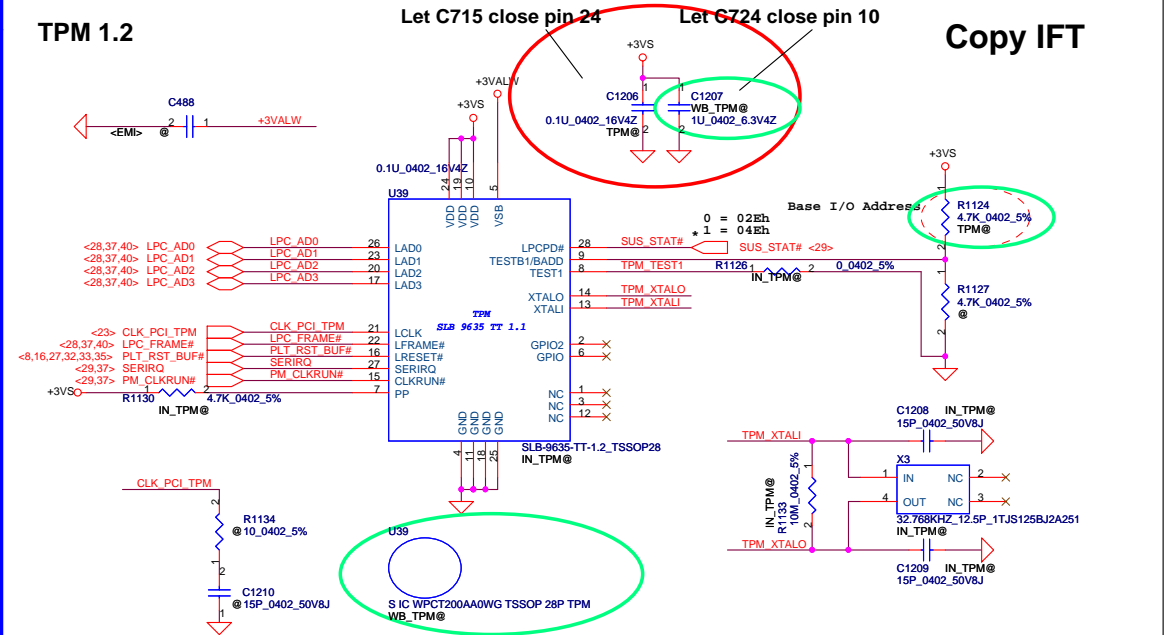
~~12/7 Modified LED footprint to LED\_HT-207UD-CB\_4P~~  
12/15 Modified to correct LED symbol!



### Camera Conn

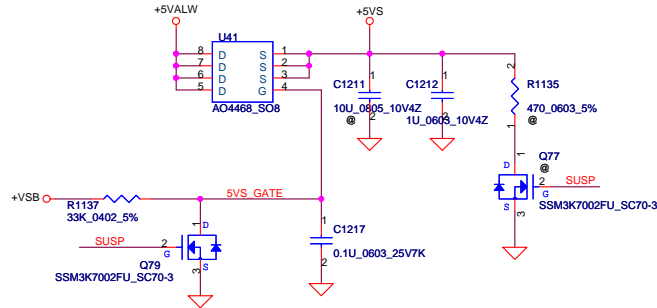


## TPM 1.2

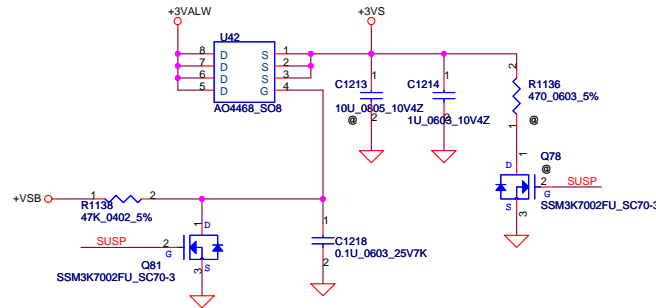


|   |                          |                    |            |                          |                 |         |
|---|--------------------------|--------------------|------------|--------------------------|-----------------|---------|
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|   |                          |                    |            | Size B                   | Document Number | Rev 1.0 |
|   |                          |                    |            | KHLBX MB Schematic       |                 |         |
| Date:   | Monday, January 19, 2009 | Sheet              | 45 of 56   |                          |                 |         |

# +5VALW TO +5VS

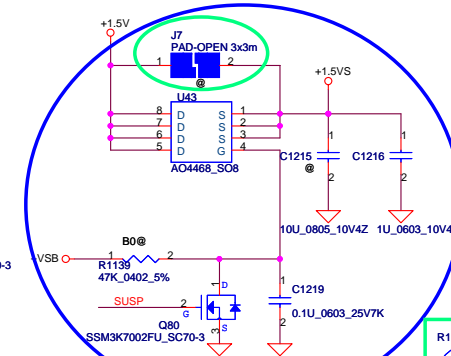


# +3VALW TO +3VS

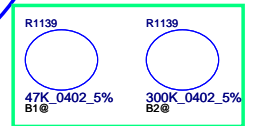


# +1.5V TO +1.5VS

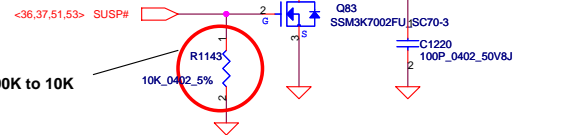
CHECK



10/22 Add by Vivian

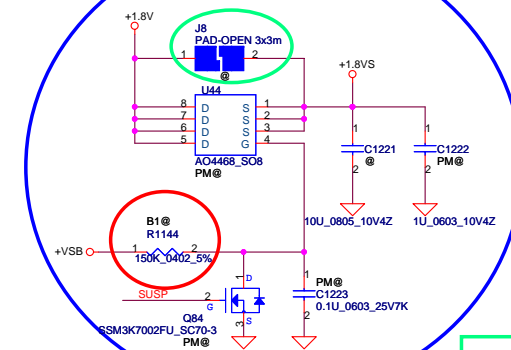


3/14 Change R16 from 100K to 10K

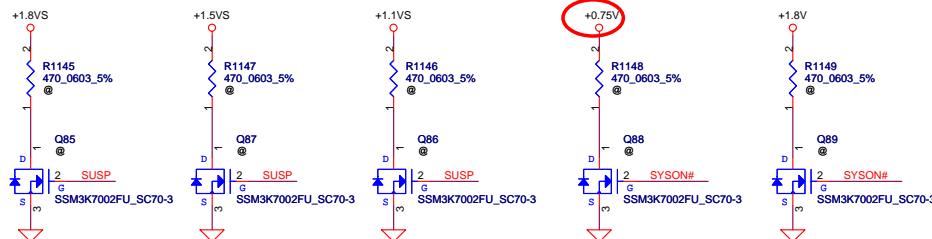
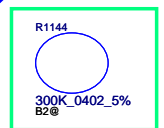


CHECK

# +1.8V TO +1.8VS

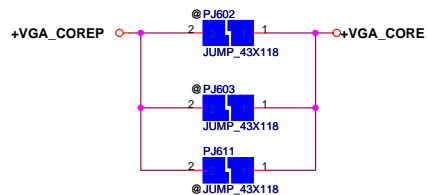
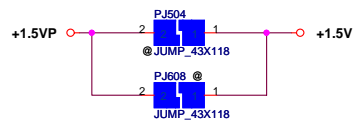
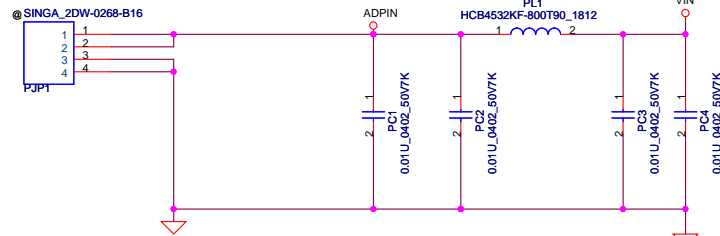


10/22 Add by Vivian

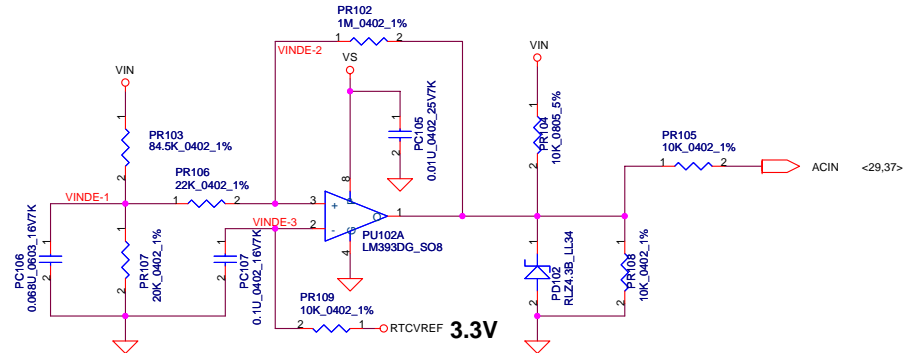
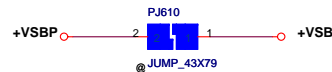


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|   |  |  |  |                          |  |  |  | DC Interface             |  |  |  |
| Size B  |  |  |  | Document Number          |  |  |  | Rev 1.0                  |  |  |  |
|   |  |  |  |                          |  |  |  | KHLBX MB Schematic       |  |  |  |
| Date:   |  |  |  | Monday, January 19, 2009 |  |  |  | Sheet 46 of 56           |  |  |  |

DC301001Y00



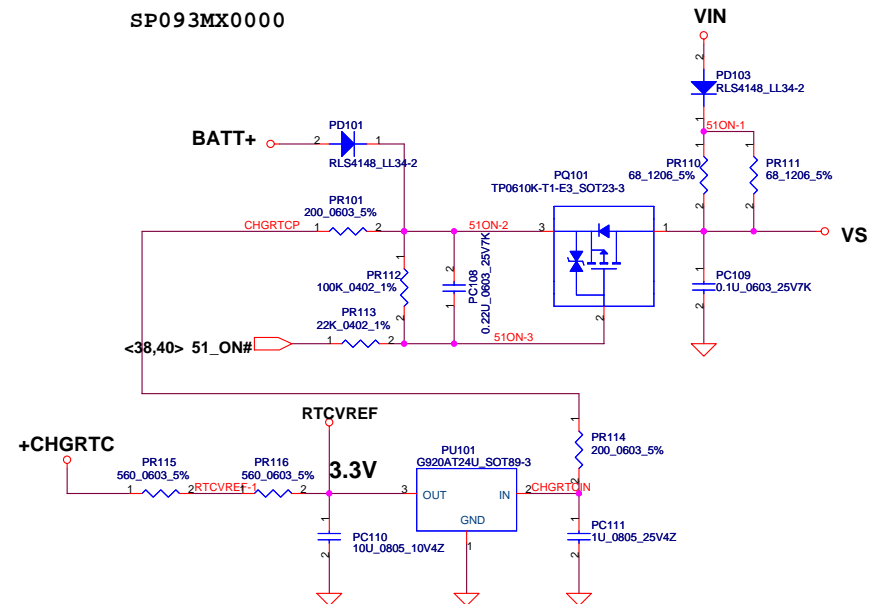
BOM structure comment  
 @ ==>unpop  
 65@==> UMA only  
 90@==>DIS only  
 NV@==>Nvidia sku only  
 M96@==>ATI sku only  
 65NV@==>UMA and NV sku only



Vin Detector

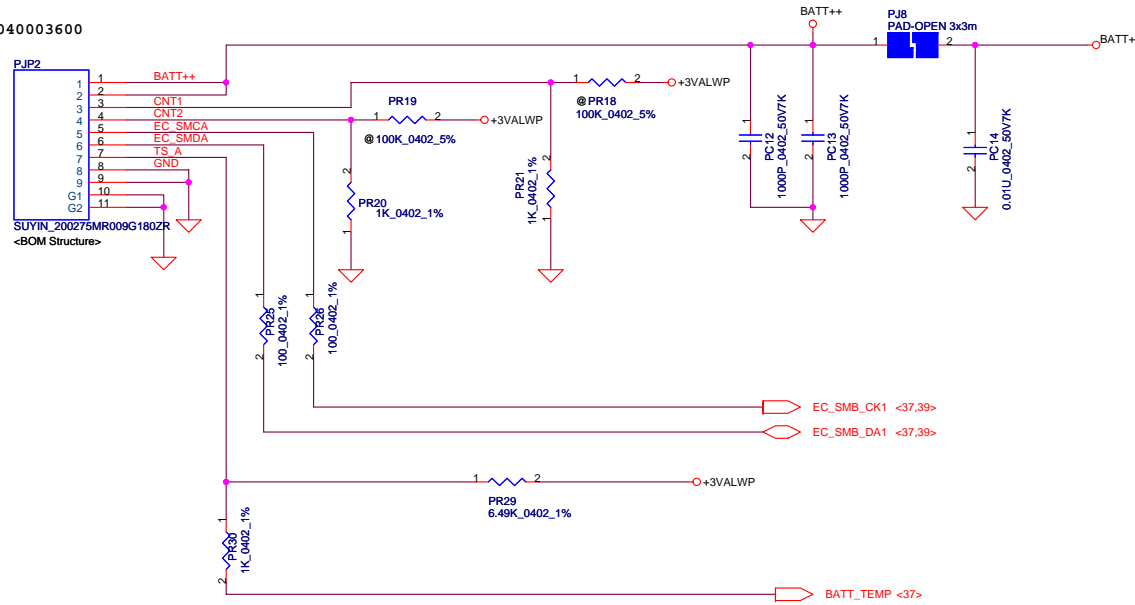
High 18.384 17.901 17.430  
 Low 17.728 17.257 16.976

SP093MX0000

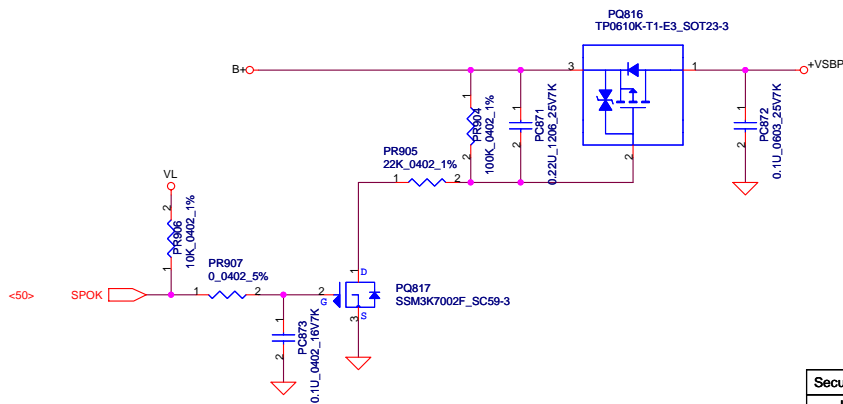
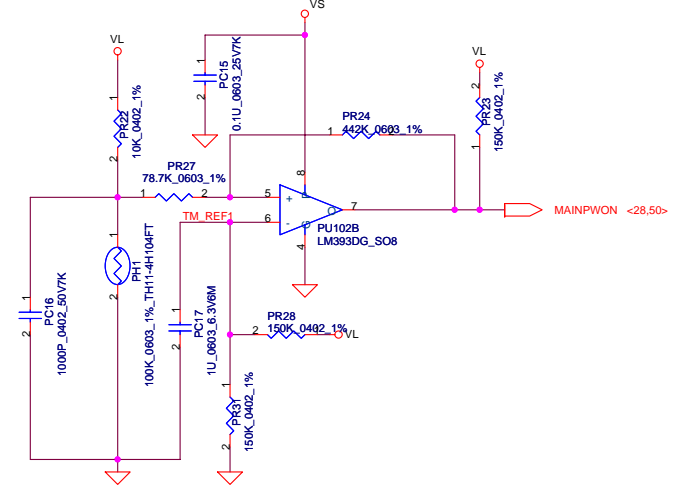


|   |                          |                    |            |                          |  |
|---|--------------------------|--------------------|------------|--------------------------|--|
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| Size  | Document Number          | KHLBX MB Schematic |            | Rev                      |  |
| Custom  |                          |                    |            | 1.0                      |  |
| Date:   | Monday, January 19, 2009 | Sheet              | 47         | of 56                    |  |

DC040003600



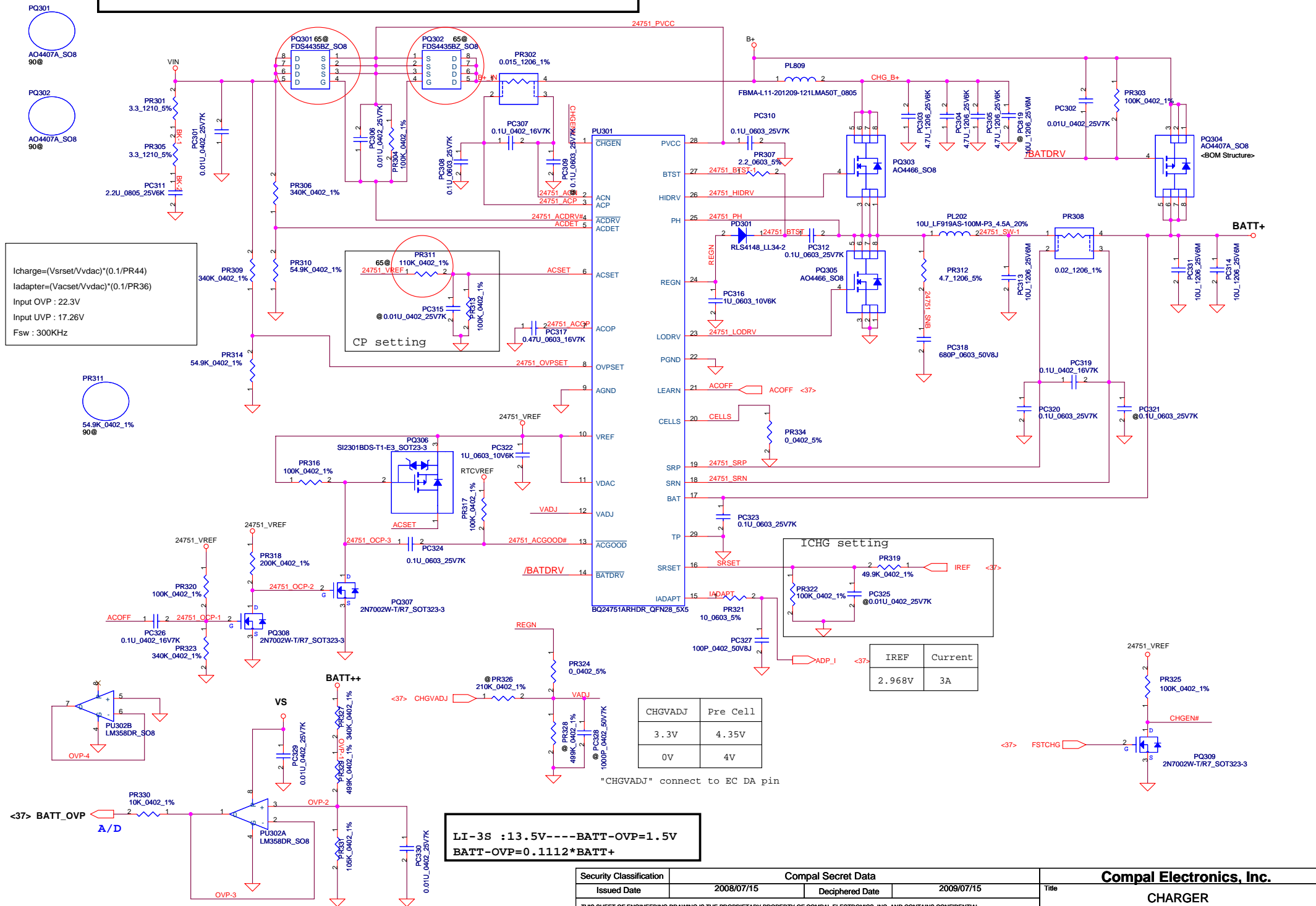
PH1 under CPU botten side :  
CPU thermal protection at 89 degree C  
Recovery at 70 degree C



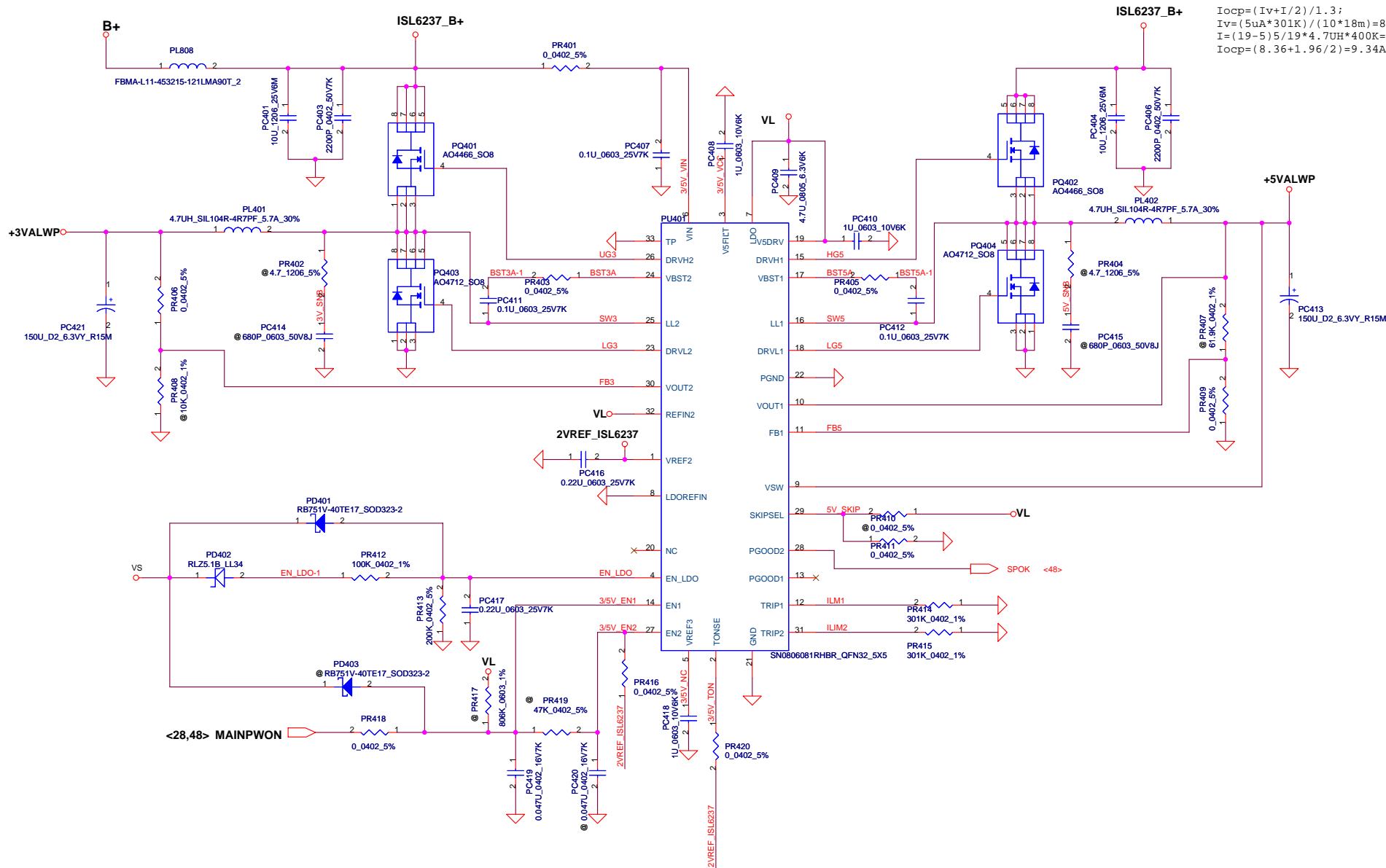
|   |            |                    |            |                          |                          |
|---|------------|--------------------|------------|--------------------------|--------------------------|
| Security Classification   |            | Compal Secret Data |            | Compal Electronics, Inc. |                          |
| Issued Date   | 2008/07/15 | Deciphered Date    | 2009/07/15 | Title                    |                          |
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|   |            |                    |            | Custom                   | KHLBX MB Schematic       |
|   |            |                    |            | Date                     | Monday, January 19, 2009 |
|   |            |                    |            | Sheet                    | 48 of 56                 |
|   |            |                    |            | Rev                      | 1.0                      |



65W, Iadapter=0~3.42A, Current sense=0.015ohm, PR45=110K, CP=3.175A  
90W, Iadapter=0~4.74A, Current Sense=0.015ohm, PR45=54.9K, CP=4.303A

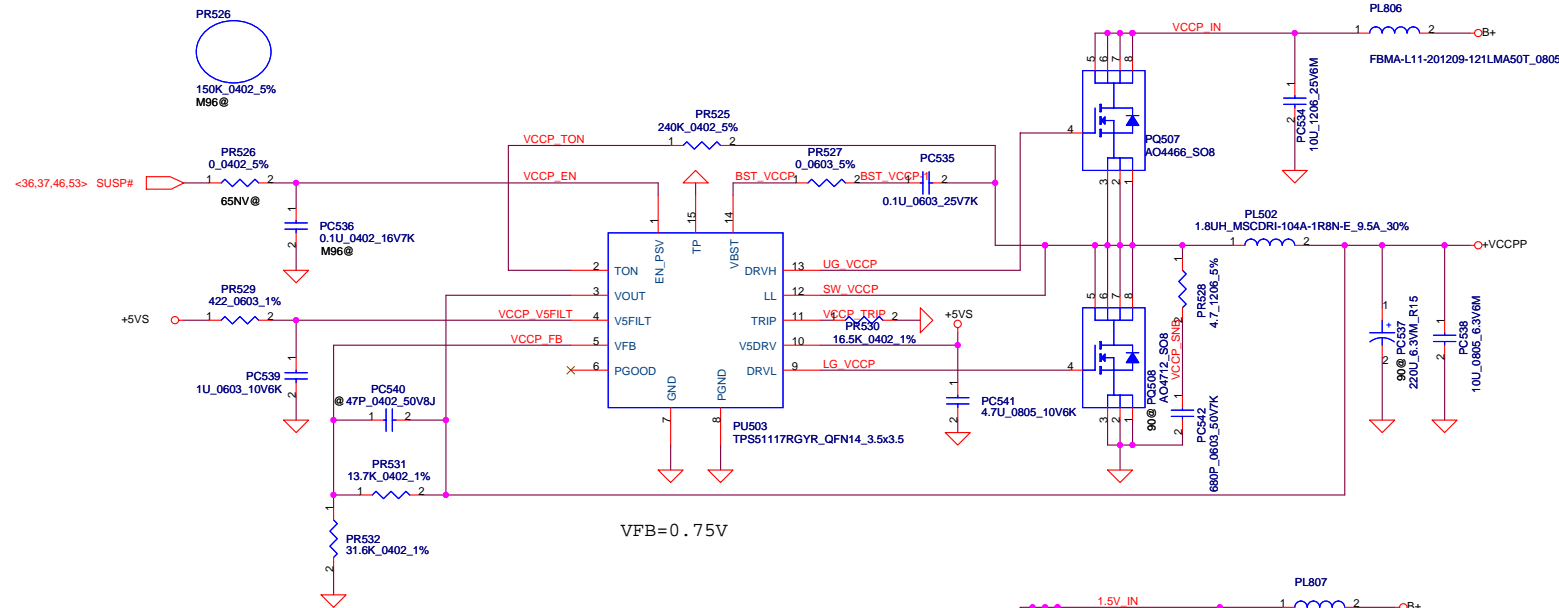


$I_{ocp} = I_v + I/2$ ;  $I_v = (5\mu A * 301K) / (10 * 18m) = 8.36A$   
 $I = (19 - 3.3) 3.3 / 19 * 4.7\mu H * 300K = 1.93A$   $I_{ocp} = 8.36 + 1.93 / 2 = 9.32A$



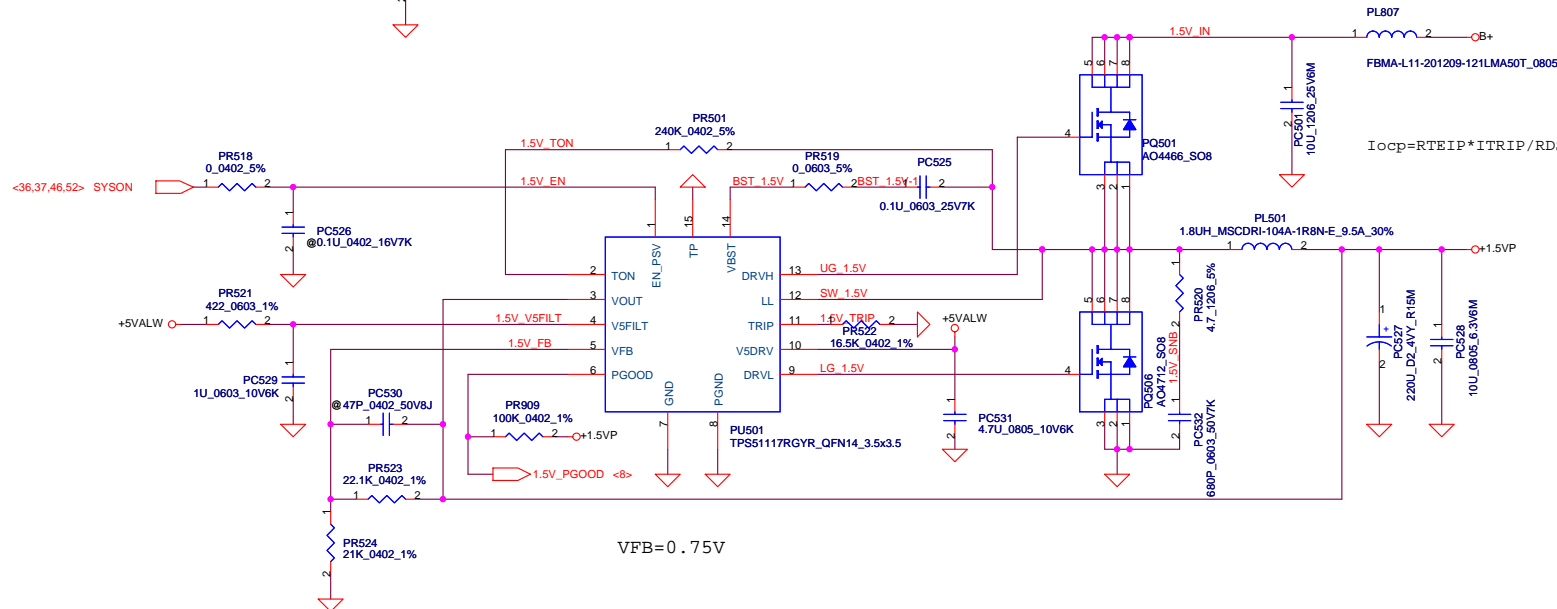
$I_{ocp} = (I_v + I/2) / 1.3$ ;  
 $I_v = (5\mu A * 301K) / (10 * 18m) = 8.36A$  ;  
 $I = (19 - 5) 5 / 19 * 4.7\mu H * 400K = 1.96A$ ;  
 $I_{ocp} = (8.36 + 1.96 / 2) = 9.34A$

|   |            |                    |            |                                |                 |
|---|------------|--------------------|------------|--------------------------------|-----------------|
| Security Classification   |            | Compal Secret Data |            | Compal Electronics, Inc.       |                 |
| Issued Date   | 2008/07/15 | Deciphered Date    | 2009/07/15 | Title                          | 3VALW/5VALW     |
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|   |            |                    |            | KHLBX MB Schematic             |                 |
|   |            |                    |            | Date: Monday, January 19, 2009 | Rev 1.0         |
|   |            |                    |            | Sheet 50                       | of 56           |



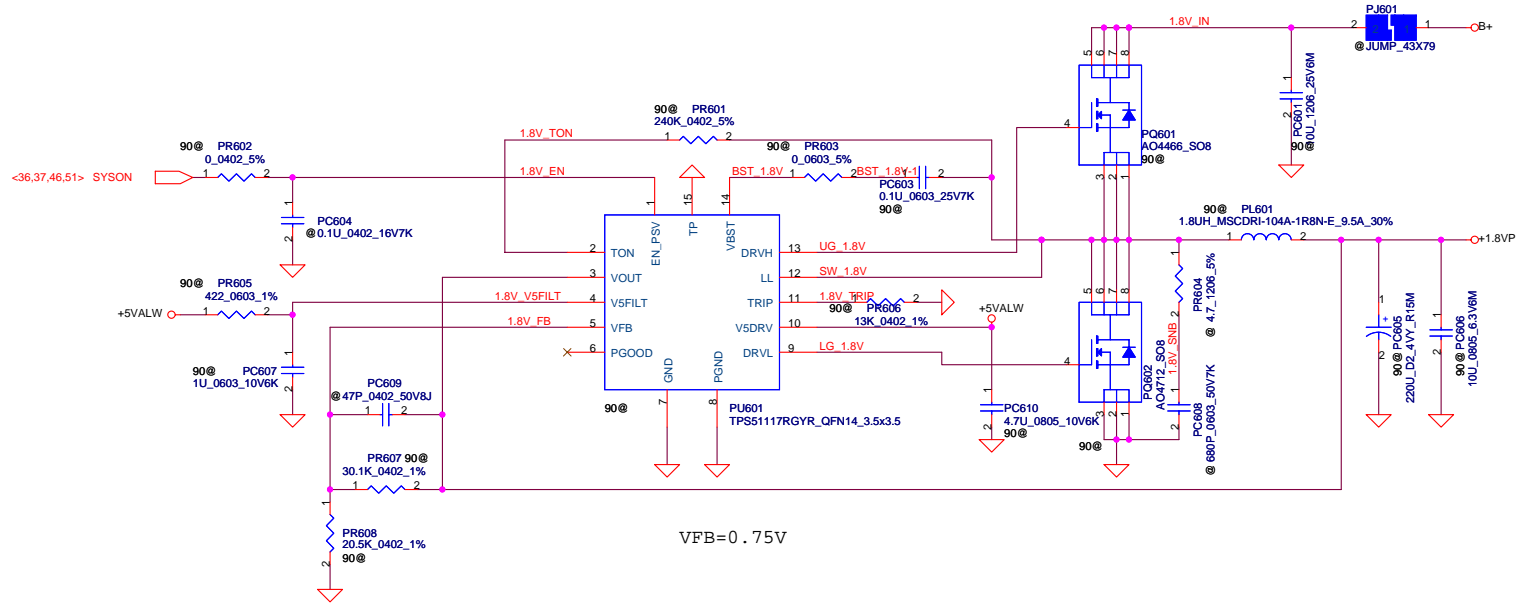
PC537  
330U 6.3V\_M  
65@

PQ508  
S TR FDS6670AS\_NL 1N SO8  
65@

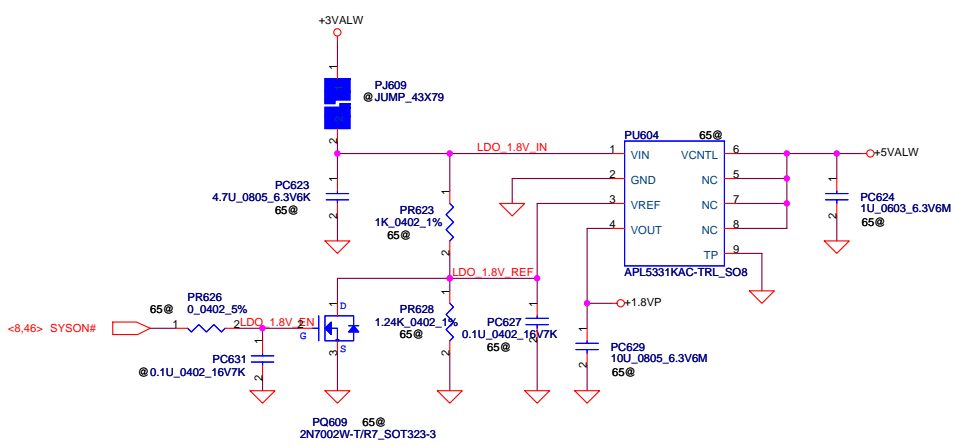
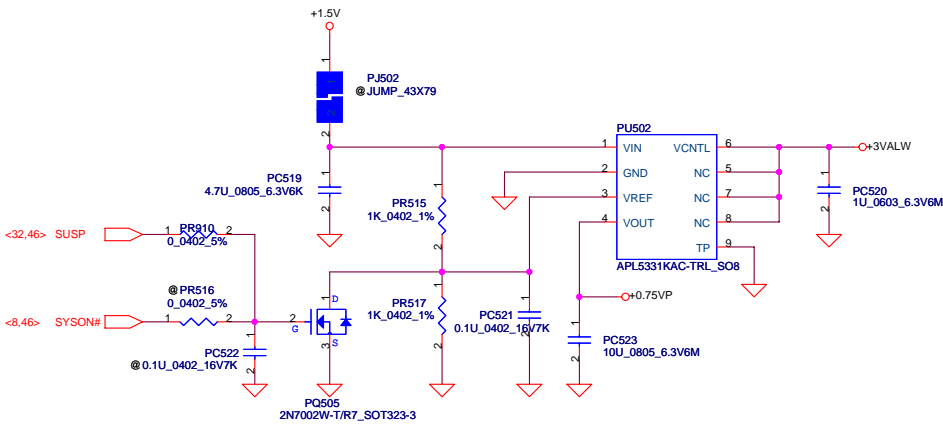


|   |            |                    |            |                                |                                    |
|---|------------|--------------------|------------|--------------------------------|------------------------------------|
| Security Classification   |            | Compal Secret Data |            | Compal Electronics, Inc.       |                                    |
| Issued Date   | 2008/07/15 | Deciphered Date    | 2009/07/15 | Title                          | 1.5V/VCCP/0.75V                    |
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|   |            |                    |            | Date: Monday, January 19, 2009 | Sheet 51 of 56                     |

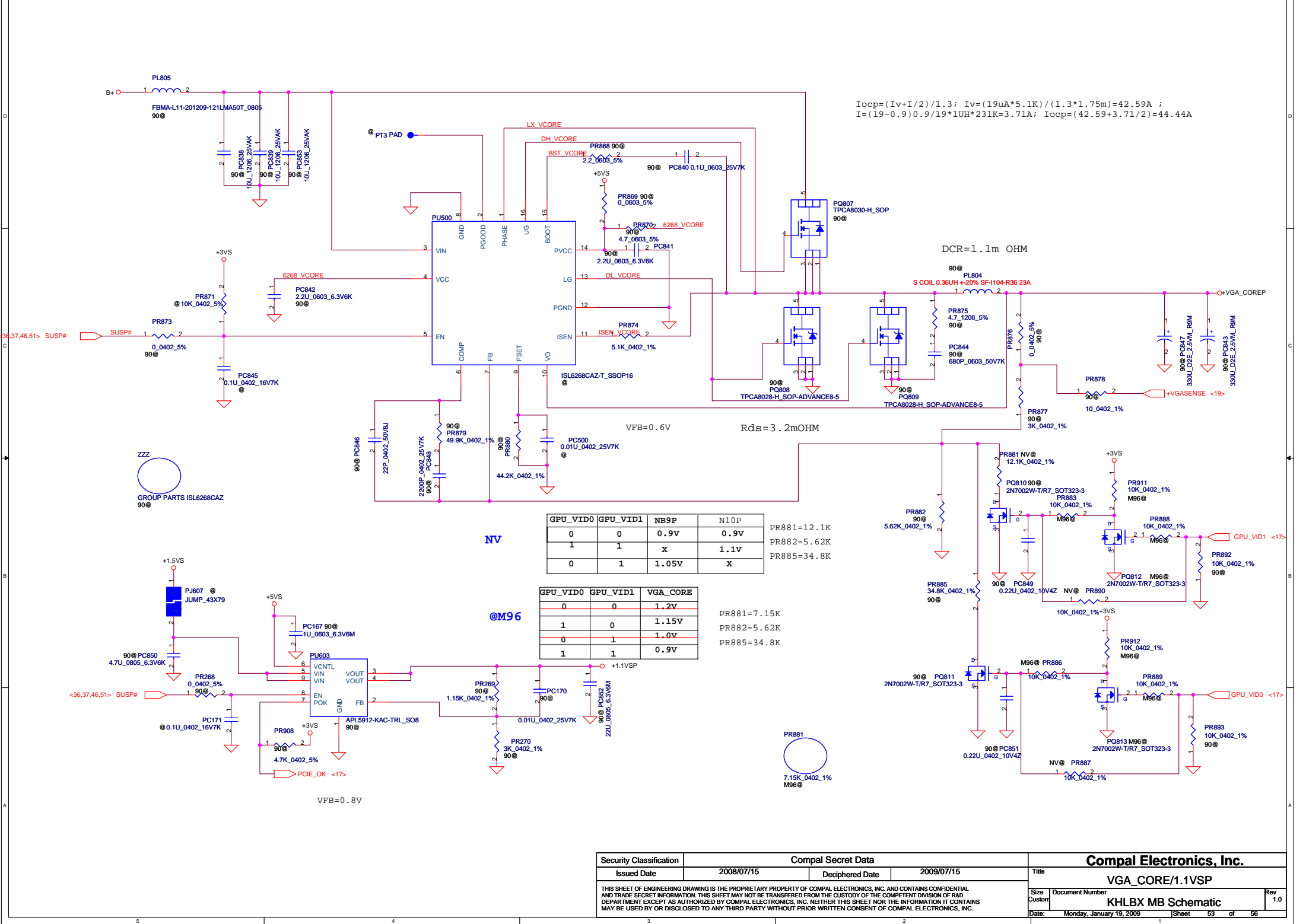
$$I_{ocp} = R_{TEIP} * I_{TRIP} / R_{DS(ON)} + 1/2 \quad I = 13k * 9u / 15m + 1/2 * 2.7 = 9.15A$$



VFB=0.75V



|   |            |                    |            |                          |  |
|---|------------|--------------------|------------|--------------------------|--|
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| Issued Date   | 2008/07/15 | Deciphered Date    | 2009/07/15 | Title                    |  |
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| Size Custom   |            | Document Number    |            | KHLBX MB Schematic       |  |
| Date: Monday, January 19, 2009  |            | Sheet 52 of 56     |            | Rev 1.0                  |  |



$I_{ocp} = (I_v + I/2) / 1.3$ ;  $I_v = (19\mu A * 5.1K) / (1.3 * 1.75m) = 42.59A$  ;  
 $I = (19 - 0.9) 0.9 / 19 * 1UH * 231K = 3.71A$ ;  $I_{ocp} = (42.59 + 3.71/2) = 44.44A$

| GPU_VID0 | GPU_VID1 | NB9P  | N10P |
|----------|----------|-------|------|
| 0        | 0        | 0.9V  | 0.9V |
| 1        | 1        | X     | 1.1V |
| 0        | 1        | 1.05V | X    |

| GPU_VID0 | GPU_VID1 | VGA_CORE |
|----------|----------|----------|
| 0        | 0        | 1.2V     |
| 1        | 0        | 1.15V    |
| 0        | 1        | 1.0V     |
| 1        | 1        | 0.9V     |





## Page

## Reason for change

## Modify list

DVT

Change Diode 4148 vendor for layout footprint

PD101,PD103,PD301

modify VGA\_core OCP to 29A

Change PR874 to 5.9K

modify VGA\_core sequence for NV and ATI

Remove PC845 &amp; change PR873 to 0 ohm

modify 1.05V sequence for ATI

Change PR526 to 150K ohm and PC536 to 0.1U

Change 2N06 to 2N7002 for costdown

PQ810 &amp; PQ811 for DIS, PQ812 &amp; PQ813 for M96

Add snubber &amp; bead at cpu\_core for EMI request

Add PR819 & PR829 to 4.7 OHM , PC815 & PC823 to 680pF,  
Change PL801 to 120 ohm bead & change PR841 & PR846 to 2.2 OHM

Add snubber &amp; bead at VGA\_core for EMI request

Add PR875 to 4.7 OHM , PC844 to 680pF,  
Change PJ605 to 120 ohm bead and change PR868 to 2.2 OHM

Add snubber &amp; bead at VCCP &amp; 1.5VP for EMI request

Add PR528 &amp; PR520 to 4.7 OHM , PC542 &amp; PC532 to 680pF

change PJ506 and PJ501 to 120 ohm bead

Add boost res. &amp; bead &amp; snubber at charger for EMI request

Change PJ301 to 120 Ohm bead and Changer PR307 to 2.2 OHM,  
Add PR312 to 4.7 Ohm & PC318 to 680P

Change 1.8UH vender to mgalaer for ZIZI nosie

PL502,PL501,PL601(DIS)

Modify 1.05V OCP for UMA(12A~19A) &amp; DIS for (8A~12A)

Change PR530 to 16.5K &amp; PQ508 to FDS6670

Modify CPU loadline

Change PR839 to 4.64K

Modify VGA CHOKE to 4mm high

PL804

Modify 1.1V to APL5912 for over loading

PU603

Change VCCP output cap to 330U for reduce ripper

PC537

Change PU500 &amp; PC500 to X76 group for 2nd

Del PU500 &amp; PC500 in 90W SKU

Add 10UF in charger output for unstable

PC331

Modify 1.5V OCP to 8A~12A

Change PR522 to 16.5K

PVT

Modify ATI VGA\_core from 1.1 to 1.15V

Change PR881 to 7.15K

Modify 220U/25V vender to SANYO from PPM suggest

Add 10UF in VGA B+ for over current(VGA B+ about 5.6A)

Add PC853 to 10U

Modify CPU loadline

Change PR839 to 4.75K

Change VGA frquency to 300K, reduce I

Change PR880to 44.2K

Change VGA FB cap for better response

Change PC848 to 2200pF

Change VGA OCP set to around 41A

Change PR874 to 8.66K

Change VGA output choke for rating.

Change PL804 to 0.36U

Add extra VGA Low Side MOS

Add PQ809

Change VGA high mos for cost down.

Change PQ807 to S TR TPCA8030-H 1N SOP-ADV

Change CPU high mos for cost down.

Change PQ801 and PQ804 to S TR TPCA8030-H 1N SOP-ADV

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Page

Reason for change

Modify list

PVT

Change VGA response

Change PR876 to 0 and PR878 to10

Change VGA OCP set

Change PR876 to 0 and PR874 to 5.1K

D

D

C

C

B

B

A

A

PVT

|   |            |                    |            |                                |   |
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